1Gb DDR3 SDRAM

Revision 0.2

Feb. 2017

Document Title

1Gb(64MX16, 128MX8, 256MX4) DDR3 SDRAM

Revision History

Revision No.	History	Draft date	Remark
0.0	Initial Draft	Feb. 12th , 2016	
0.1	Updated IDD Specifications	Jan. 4th , 2017	
0.2	Updated IDD Specifications of x4 and x8	Feb. 21st , 2017	

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DDR3 Sync DRAM Features

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  - 1.5V center-terminated push/pull I/O
  - 8n-bit prefetch DDR architecture
  - Differential clock inputs (CK, CK#)
  - 8 internal banks
  - Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
  - Differential data strobe per byte of data(DQS/DQS#).
  - DM masks write date at the both rising and falling edge of the data strobe
  - Programmable CAS READ latency (CL)
  - Posted CAS additive latency
  - Programmable CAS WRITE latency (CWL) based on tCK
  - Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
  - Selectable BC4 or BL8 on–the-fly (OTF)
  - Self refresh mode
  - Tc of 0℃ to +95℃
    - · 64ms, 8192 cycle refresh at 0℃ to +85℃
    - · 32ms, 8192 cycle refresh at 85℃ to +95℃
  - Self refresh temperature (SRT)
  - Automatic self refresh (ASR)
  - Write leveling
  - Multipurpose register
  - Output driver calibration
- **Configuration**
  - 64 Meg X 16 (8 Meg X 16 X 8 Banks).
  - 128 Meg X 8 (16 Meg X 8 X 8 Banks)
  - 256 Meg X 4 (32 Meg X 4 X 8 Banks)
- **Timing – Cycle time**
  - 938ps @ CL = 14 (-AN)
  - 1.07ns @ CL = 13 (-9M)
  - 1.25ns @ CL = 11 (-8K)
  - 1.50ns @ CL = 9 (-6H)
  - 1.87ns @ CL = 7 (-5F)
- **Operating Temperature Ranges**
  - Commercial (0℃ to +95℃)
  - Industrial (-40℃ to +95℃)

Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)	Notes
-AN	2133	14-14-14	13.09	13.09	13.09	1, 2, 3, 4
-9M	1866	13-13-13	13.91	13.91	13.91	1, 2, 3
-8K	1600	11-11-11	13.75	13.75	13.75	1, 2
-6H	1333	9-9-9	13.5	13.5	13.5	1
-5F	1066	7-7-7	13.1	13.1	13.1	

Notes : 1. Backward compatible to 1066, CL = 7.
2. Backward compatible to 1333, CL = 9.
3. Backward compatible to 1600, CL = 11.
4. Backward compatible to 1866, CL = 13.

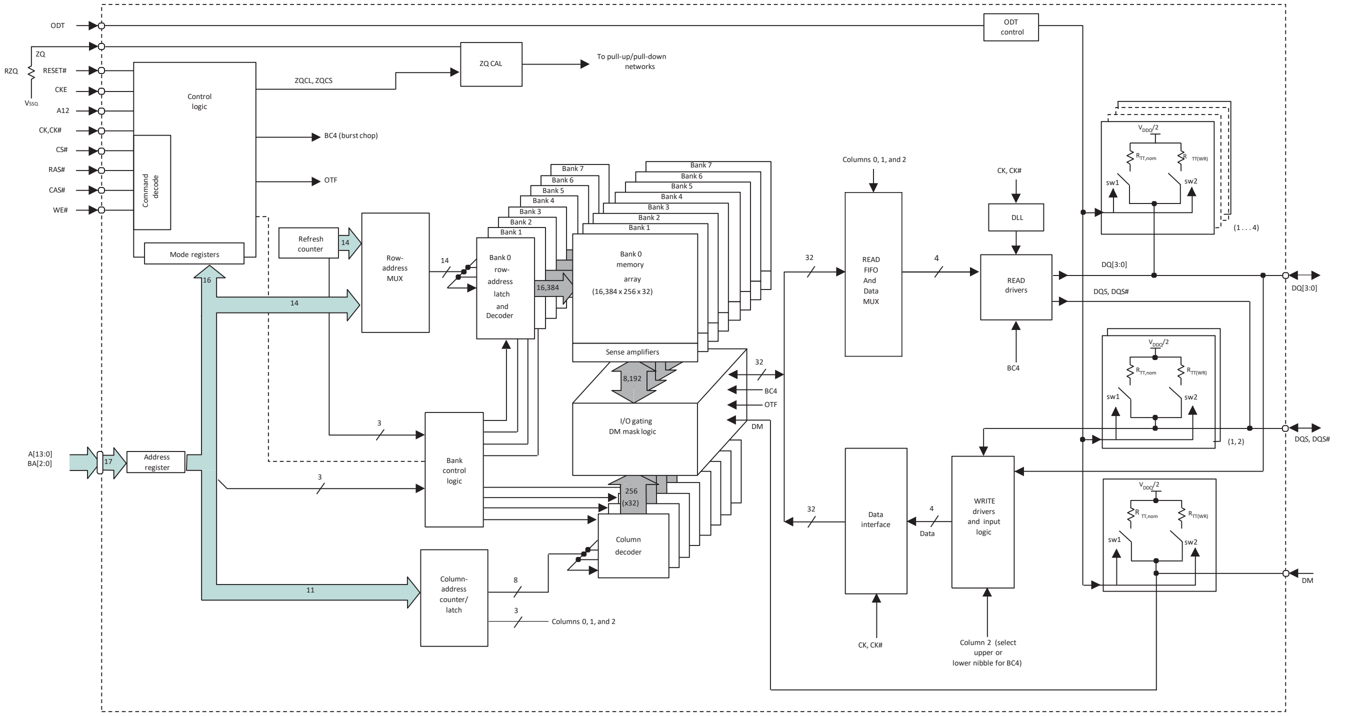
Addressing

Parameter	256 Meg x 4	128 Meg x 8	64 Meg x 16
Configuration	32 Meg x 4 x 8 banks	16 Meg x 8 x 8 banks	8 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row addressing	16K (A[13:0])	16K (A[13:0])	8K (A[12:0])
Bank addressing	8 (BA[2:0])	8 (BA[2:0])	8 (BA[2:0])
Column addressing	2K (A[11, 9:0])	1K (A[9:0])	1K (A[9:0])
Page Size	1KB	1KB	2KB

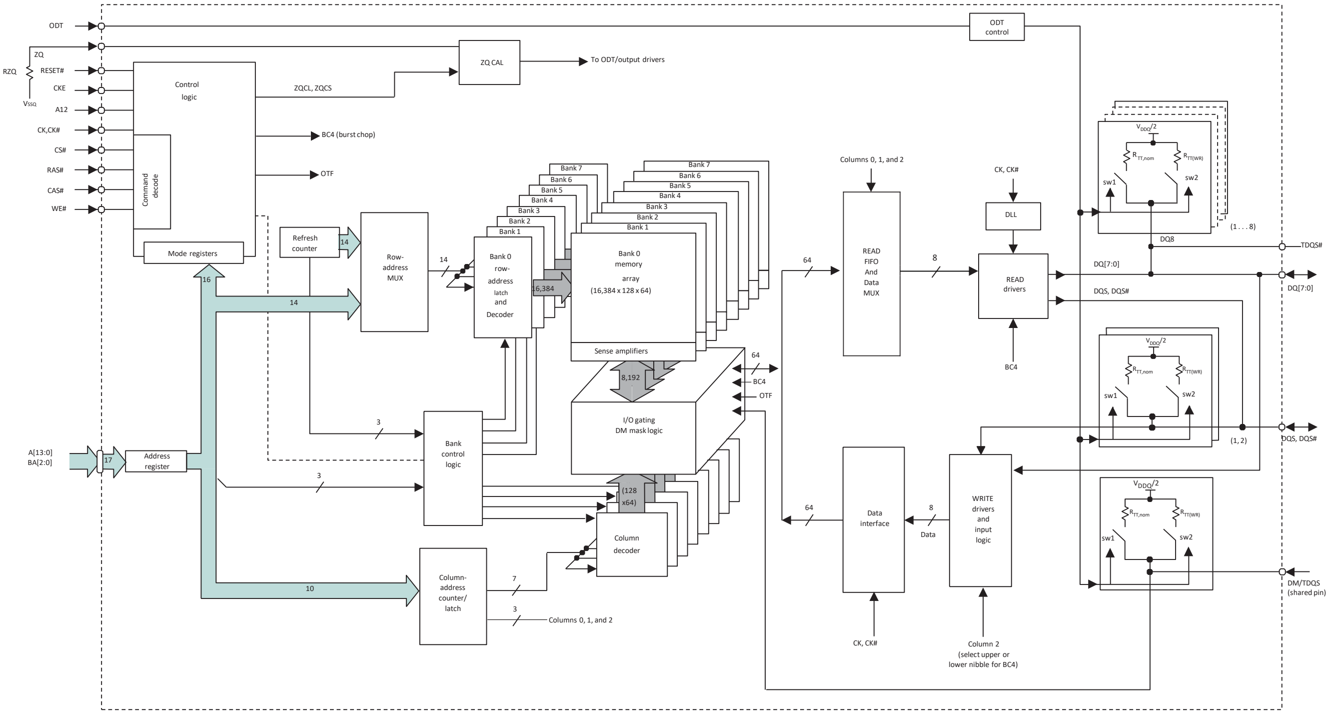
Functional Block Diagrams

DDR3 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 8-bank DRAM.

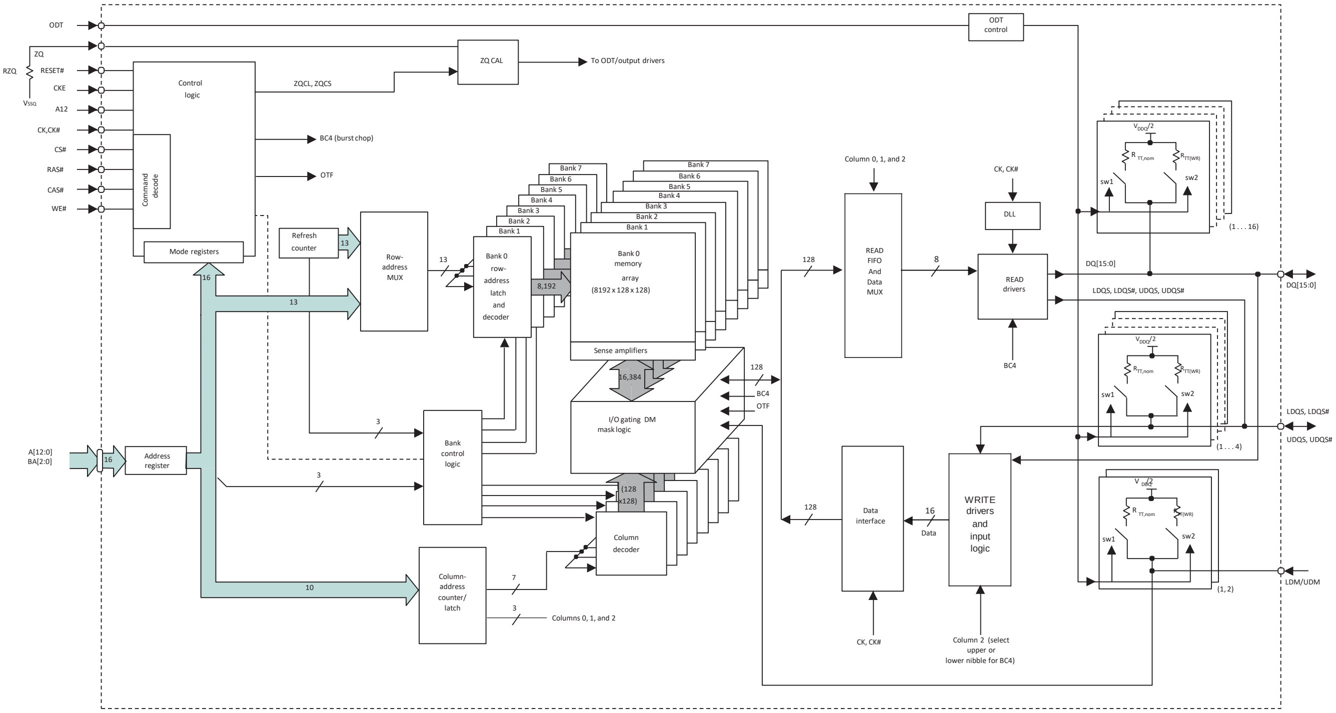
256 Meg x 4 Functional Block Diagram



128 Meg x 8 Functional Block Diagram

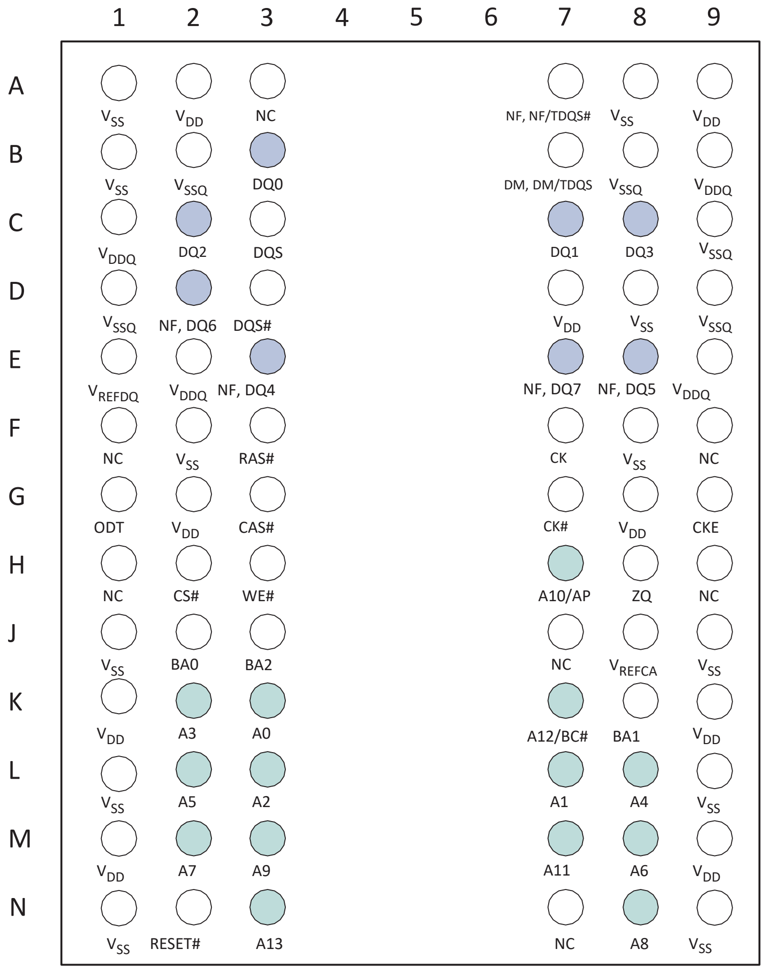


64 Meg x 16 Functional Block Diagram



Ball Assignments and Descriptions

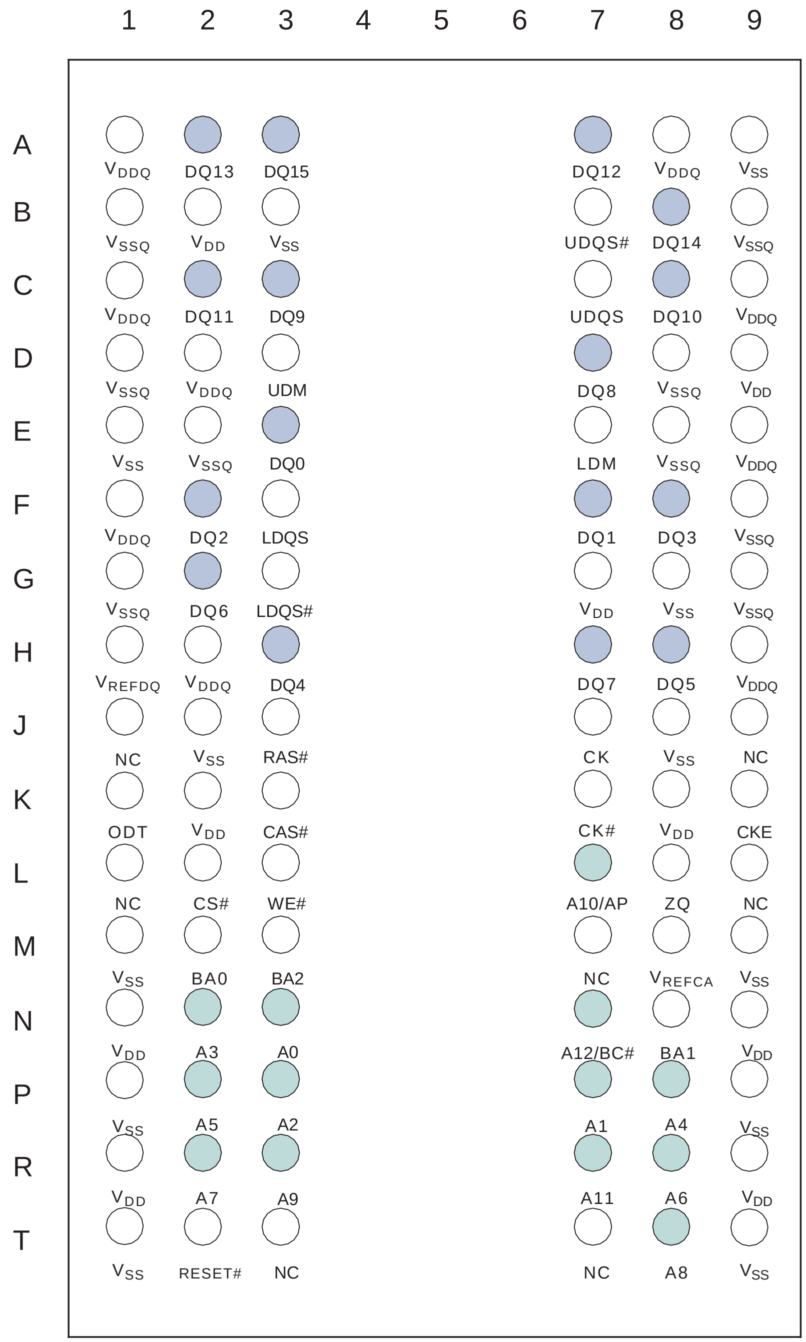
78-Ball FBGA – x4, x8 (Top View)



	1	2	3	4	5	6	7	8	9
A	V_{SS}	V_{DD}	NC				NF, NF/TDQS#	V_{SS}	V_{DD}
B	V_{SS}	V_{SSQ}	DQ0				DM, DM/TDQS	V_{SSQ}	V_{DDQ}
C	V_{DDQ}	DQ2	DQS				DQ1	DQ3	V_{SSQ}
D	V_{SSQ}	NF, DQ6	DQS#				V_{DD}	V_{SS}	V_{SSQ}
E	V_{REFDQ}	V_{DDQ}	NF, DQ4				NF, DQ7	NF, DQ5	V_{DDQ}
F	NC	V_{SS}	RAS#				CK	V_{SS}	NC
G	ODT	V_{DD}	CAS#				CK#	V_{DD}	CKE
H	NC	CS#	WE#				A10/AP	ZQ	NC
J	V_{SS}	BA0	BA2				NC	V_{REFCA}	V_{SS}
K	V_{DD}	A3	A0				A12/BC#	BA1	V_{DD}
L	V_{SS}	A5	A2				A1	A4	V_{SS}
M	V_{DD}	A7	A9				A11	A6	V_{DD}
N	V_{SS}	RESET#	A13				NC	A8	V_{SS}

Notes :
1. Ball descriptions listed in Table(page 20) are listed as “x4, x8” if unique; otherwise, x4 and x8 are the same.
2. A comma separates the configuration; a slash defines a selectable function.
   Example A7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only selectable between NF or TDQS# via MRS (symbols are defined in Ball description).

96-Ball FBGA – x16 (Top View)

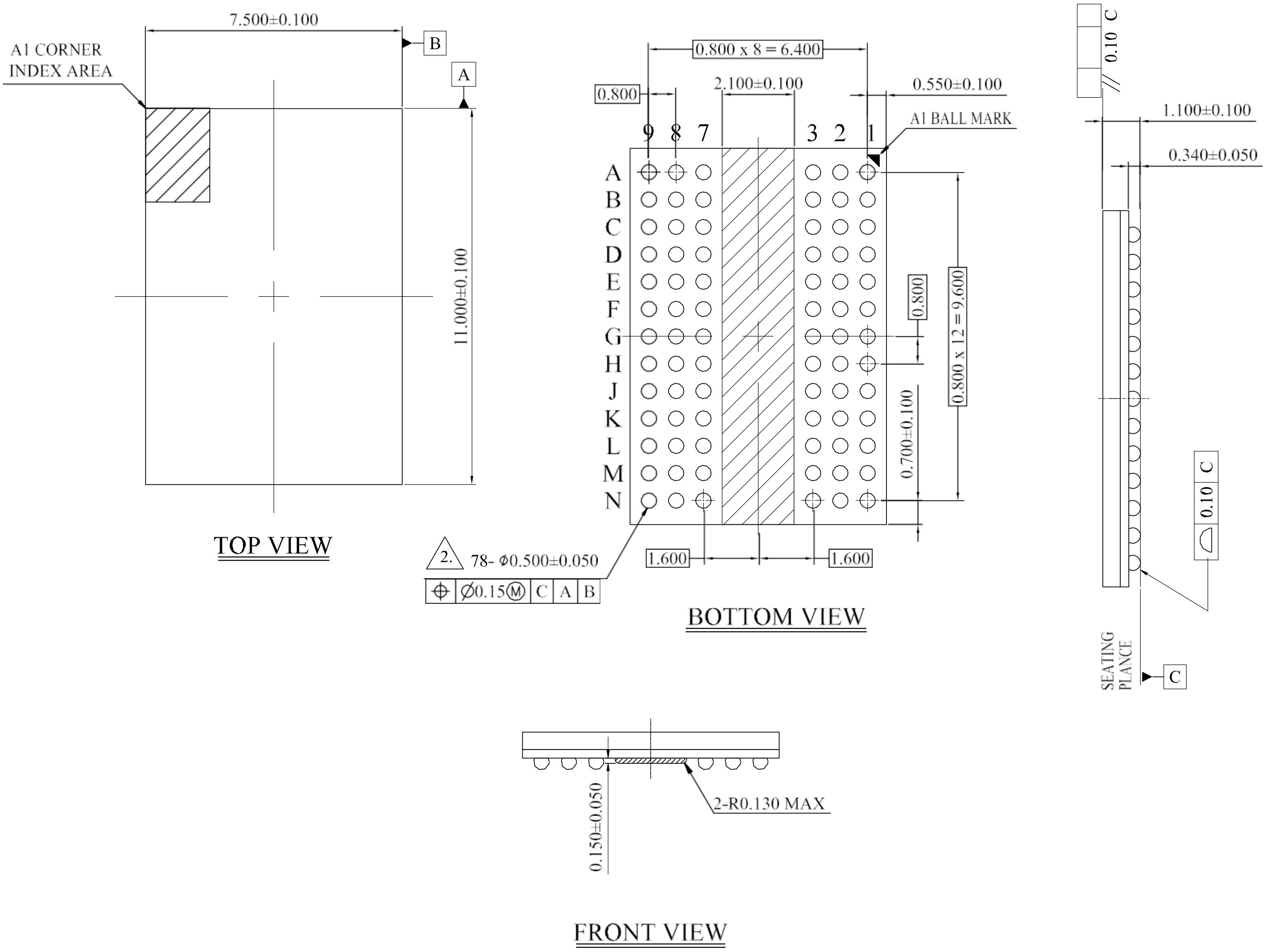


	1	2	3	4	5	6	7	8	9
A	V_{DDQ}	DQ13	DQ15				DQ12	V_{DDQ}	V_{SS}
B	V_{SSQ}	V_{DD}	V_{SS}				UDQS#	DQ14	V_{SSQ}
C	V_{DDQ}	DQ11	DQ9				UDQS	DQ10	V_{DDQ}
D	V_{SSQ}	V_{DDQ}	UDM				DQ8	V_{SSQ}	V_{DD}
E	V_{SS}	V_{SSQ}	DQ0				LDM	V_{SSQ}	V_{DDQ}
F	V_{DDQ}	DQ2	LDQS				DQ1	DQ3	V_{SSQ}
G	V_{SSQ}	DQ6	LDQS#				V_{DD}	V_{SS}	V_{SSQ}
H	V_{REFDQ}	V_{DDQ}	DQ4				DQ7	DQ5	V_{DDQ}
J	NC	V_{SS}	RAS#				CK	V_{SS}	NC
K	ODT	V_{DD}	CAS#				CK#	V_{DD}	CKE
L	NC	CS#	WE#				A10/AP	ZQ	NC
M	V_{SS}	BA0	BA2				NC	V_{REFCA}	V_{SS}
N	V_{DD}	A3	A0				A12/BC#	BA1	V_{DD}
P	V_{SS}	A5	A2				A1	A4	V_{SS}
R	V_{DD}	A7	A9				A11	A6	V_{DD}
T	V_{SS}	RESET#	NC				NC	A8	V_{SS}

Notes : 1. Ball descriptions listed in Table (page 22).

Package Dimensions

78-Ball FBGA – x4, x8



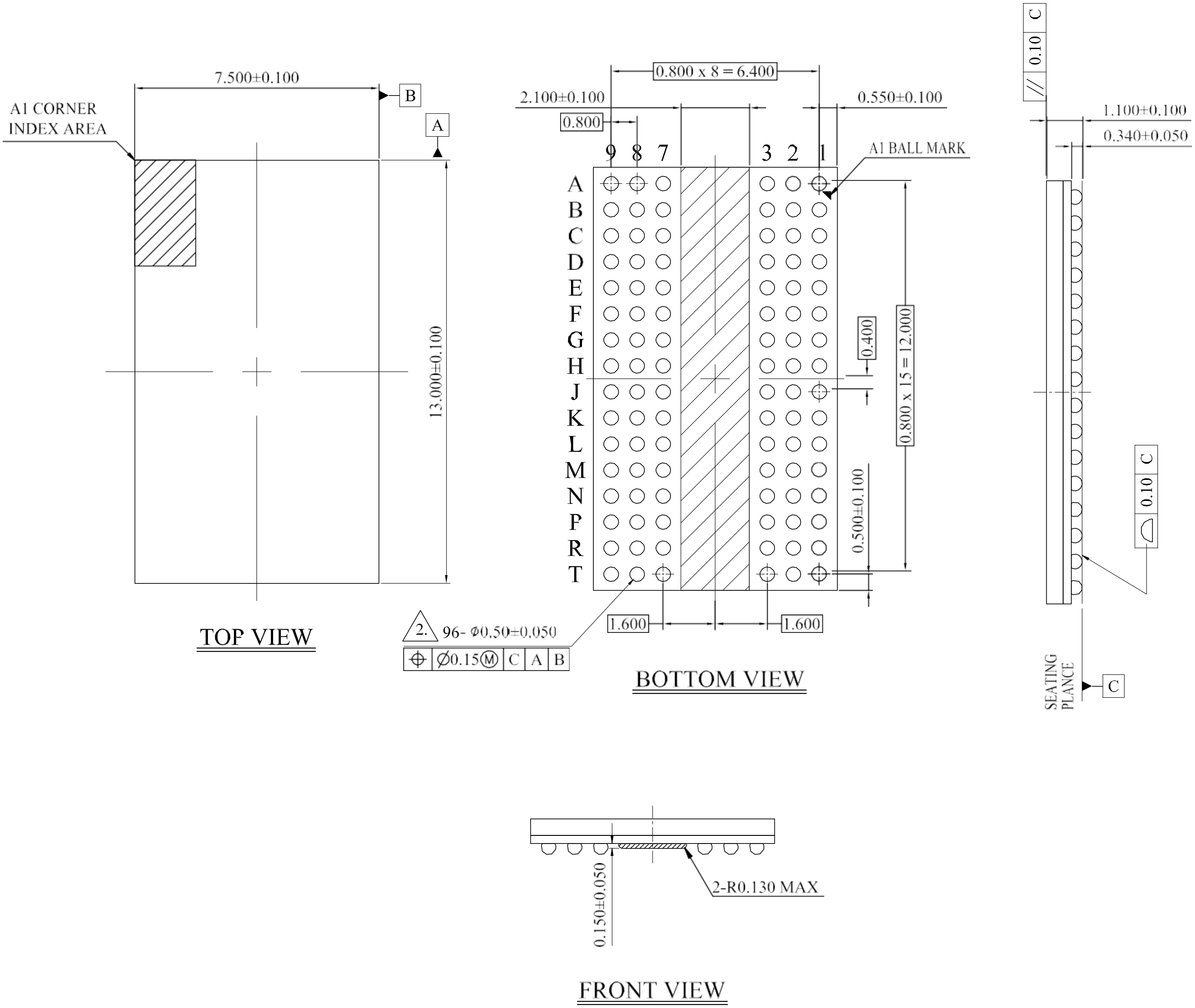
TOP VIEW

BOTTOM VIEW

FRONT VIEW

Notes : 1. All dimensions are in millimeters.
②. Post-Reflow solder ball Diameters. (Pre-Reflow Diameter : Ø0.45 ± 0.2)

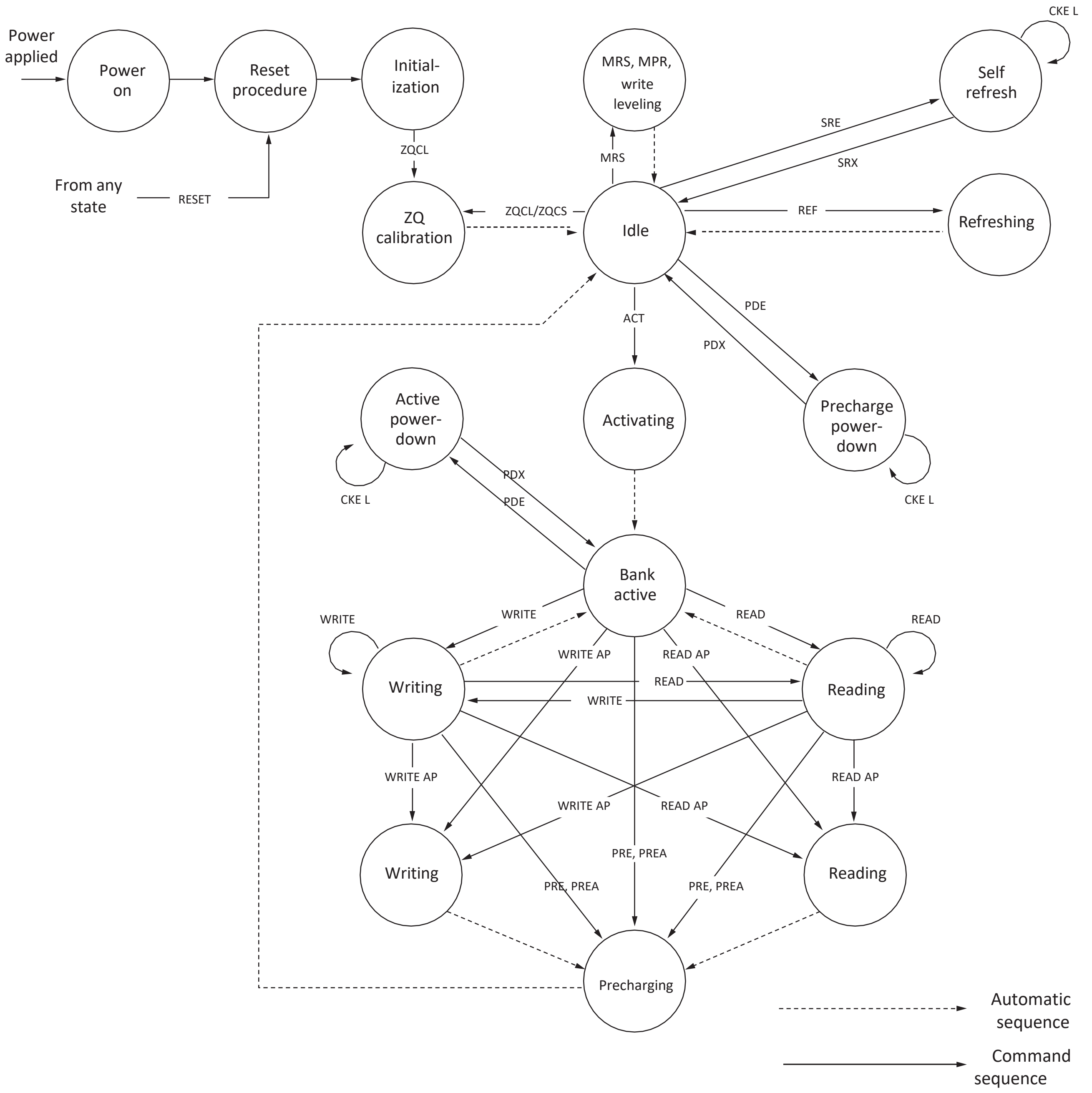
96-Ball FBGA – x16



Notes : 1. All dimensions are in millimeters.

②. Post-Reflow solder ball Diameters. (Pre-Reflow Diameter : Ø0.45 ± 0.2)

Simplified Bus Interface State Diagram



ACT = Activate
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = Precharge

PREA = Precharge all
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8 REF = Refresh
RESET = Start reset procedure
SRE = Self refresh entry

SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8 ZQCL = ZQ long calibration
ZQCS = ZQ short calibration

78-Ball FBGA – x4, x8 Ball Descriptions

Symbol	Type	Description
A13, A12/BC# A10/AP, A[9:0]	Input	**Address inputs :** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to VREFCA. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH=BL8 or no burst chop, LOW=BC4).
BA [2:0]	Input	**Bank address inputs :** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to VREFCA.
CK, CK#	Input	**Clock :** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable :** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled / disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to VREFCA.
CS#	Input	**Chip select :** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to VREFCA.
DM	Input	**Input data mask :** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to VREFDQ. DM has an optional use as TDQS on the x8.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to VREFCA.
RAS#, CAS#, WE#	Input	**Command inputs :** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to VREFCA.
RESET#	Input	**Reset :** RESET# is an active LOW CMOS input referenced to VSS. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × VDD and DC LOW ≤ 0.2 × VDDQ. RESET# assertion and desertion are asynchronous.
DQ[3:0]	I/O	**Data input/output:** Bidirectional data bus for the x4 configuration. DQ[3:0] are referenced to VREFDQ.
DQ[7:0]	I/O	**Data input/output:** Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to VREFDQ.

78-Ball FBGA – x4, x8 Ball Descriptions (Continued)

Symbol	Type	Description
DQS, DQS#	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
TDQS, TDQS#	Output	**Termination data strobe:** Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
VDD	Supply	**Power supply:** 1.5V ±0.075V.
VDDQ	Supply	**DQ power supply:** 1.5V ±0.075V. Isolated on the device for improved noise immunity.
VREFCA	Supply	**Reference voltage for control, command, and address:** VREFCA must be maintained at all times (including self refresh) for proper device operation.
VREFDQ	Supply	**Reference voltage for data:** VREFDQ must be maintained at all times (excluding self refresh) for proper device operation.
VSS	Supply	Ground.
VSSQ	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to VSSQ.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
NF	–	**No function:** When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

96-Ball FBGA – x16 Ball Descriptions

Symbol	Type	Description
A12/BC#, A10/AP, A[9:0]	Input	**Address inputs :** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to VREFCA. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH=BL8 or no burst chop, LOW=BC4).
BA [2:0]	Input	**Bank address inputs :** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to VREFCA.
CK, CK#	Input	**Clock :** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable :** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled /disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle),or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to VREFCA.
CS#	Input	**Chip select :** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to VREFCA.
LDM	Input	**Input data mask :** LDM is a lower-byte, input mask signal for write data. Lower-byte input data is masked when LDM is sampled HIGH along with the input data during a write access. Although the LDM ball is input-only, the LDM loading is designed to match that of the DQ and DQS balls. LDM is referenced to VREFDQ.
ODT	Input	**On-die termination :** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM for the x16; DQ0[7:0], DQS, DQS# DM /TDQS, and NF/TDQS# (when TDQS is enabled) for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to VREFCA.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to VREFCA.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to VSS. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × VDD and DC LOW ≤ 0.2 × VDDQ. RESET# assertion and desertion are asynchronous..

96-Ball FBGA – x16 Ball Descriptions

Symbol	Type	Description
UDM	input	**Input data mask :** UDM is an upper-byte, input mask signal for write data. Upper byte input data is masked when UDM is sampled HIGH along with that input data during a WRITE access. Although the UDM ball is input-only, the UDM loading is designed to match that of the DQ and DQS balls. UDM is referenced to VREFDQ.
DQ[7:0]	I/O	**Data input/output :** Lower byte of bidirectional data bus for the x16 configuration. DQ[7:0] are referenced to VREFDQ.
DQ[15:8]	I/O	**Data input/output :** Upper byte of bidirectional data bus for the x16 configuration. DQ[15:8] are referenced to VREFDQ.
LDQS, LDQS#	I/O	**Lower byte data strobe :** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
UDQS, UDQS#	I/O	**Upper byte data strobe :** Output with read data. Edge-aligned with read data. Input with write data. DQS is center-aligned to write data..
VDD	Supply	**Power supply :** 1.5V ±0.075V.
VDDQ	Supply	**DQ power supply :** 1.5V ±0.075V. Isolated on the device for improved noise immunity.
VREFCA	Supply	**Reference voltage for control, command, and address :** VREFCA must be maintained at all times (including self refresh) for proper device operation.
VREFDQ	Supply	**Reference voltage for data :** VREFDQ must be maintained at all times (excluding self refresh) for proper device operation.
VSS	Supply	Ground.
VSSQ	Supply	**DQ ground :** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration :** This ball is tied to an external 240Ω resistor (RZQ), which is tied to VSSQ.
NC	–	**No connect :** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

Functional Description

DDR3 SDRAM uses a double data rate architecture to achieve high-speed operation.
The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM effectively consists of a single 8*n*-bit-wide, four-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The DDR3 SDRAM operates from a differential clock (CK and CK#). The crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

Read and write accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access.

The device uses a READ and WRITE BL8 and BC4. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

Industrial Temperature

The industrial temperature (IT) device requires that the case temperature not exceed –40°C or 95°C. JEDEC specifications require the refresh rate to double when TC exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when TC is < 0°C or >95°C.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation).
- Throughout this data sheet, various figures and text refer to DQs as “DQ.” DQ is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms “DQS” and “CK” found throughout this data sheet are to be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise.
- Complete functionality may be described throughout the document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated is considered undefined, illegal, and not supported, and can result in unknown operation.

- Row addressing is denoted as A[*n*:0]. *For example,* 1Gb: *n* = 12 (x16); 1Gb: *n* = 13 (x4, x8); 2Gb: *n* = 13 (x16) and 2Gb : *n* = 14 (x4, x8); 4Gb: *n* = 14 (x16); and 4Gb: *n* = 15 (x4, x8).
- Dynamic ODT has a special use case: when DDR3 devices are architected for use in a single rank memory array, the ODT ball can be wired HIGH rather than routed.
  Refer to the Dynamic ODT Special Use Case section.
- A x16 device's DQ bus is comprised of two bytes. If only one of the bytes needs to be used, use the lower byte for data transfers and terminate the upper byte as noted :
  - Connect UDQS to ground via 1kΩ* resistor.
  - Connect UDQS# to VDD via 1kΩ* resistor.
  - Connect UDM to VDD via 1kΩ* resistor.
  - Connect DQ[15:8] individually to either VSS, VDD, or VREF via 1kΩ resistors,* or float DQ[15:8].

* If ODT is used, 1kΩ resistor should be changed to 4x that of the selected ODT.

Electrical Specifications

Absolute Ratings

Stresses greater than those listed in Table 1 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 1 : Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V	1
V_{DDQ}	V_{DD} supply voltage relative to V_{SSQ}	–0.4	1.975	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.975	V	
T_C	Operating case temperature - Commercial	0	95	°C	2, 3
	Operating case temperature - Industrial	–40	95	°C	2, 3
	Operating case temperature - Automotive	–40	105	°C	2, 3
T_{STG}	Storage temperature	–55	150	°C	

Notes :
1. VDD and VDDQ must be within 300mV of each other at all times, and VREF must not be greater than 0.6 × VDDQ. When VDD and VDDQ are <500mV, VREF can be ≤300mV.
2. MAX operating case temperature. TC is measured in the center of the package.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum TC during operation.

Input / Output Capacitance

Table 2 : DDR3 Input / Output Capacitance

Note 1 applies to the entire table

Capacitance Parameters	Symbol	800		1066		1333		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CK and CK#	C_{CK}	0.8	1.6	0.8	1.6	0.8	1.4	pF	
ΔC: CK to CK#	C_{DCK}	0	0.15	0	0.15	0	0.15	pF	
Single-end I/O : DQ, DM	C_{IO}	1.5	3	1.5	2.7	1.5	2.5	pF	2
Differential I/O : DQS, DQS#, TDQS, TDQS#	C_{IO}	1.5	3	1.5	2.7	1.5	2.5	pF	3
ΔC: DQS to DQS#,TDQS, TDQS#	C_{DDQS}	0	0.2	0	0.2	0	0.15	pF	3
ΔC: DQ to DQS	C_{DIO}	–0.5	0.3	–0.5	0.3	–0.5	0.3	pF	4
Inputs(CTRL, CMD, ADDR)	C_{I}	0.75	1.4	0.75	1.35	0.75	1.3	pF	5
ΔC: CTRL to CK	C_{DI_CTRL}	–0.5	0.3	–0.5	0.3	–0.4	0.2	pF	6
ΔC: CMD_ADDR to CK	$C_{DI\_CMD\_ADDR}$	–0.5	0.5	–0.5	0.5	–0.4	0.4	pF	7
ZQ pin capacitance	C_{ZQ}	–	3.0	–	3.0	–	3.0	pF	
Reset pin capacitance	C_{RE}	–	3.0	–	3.0	–	3.0	pF	

Capacitance Parameters	Symbol	1600		1866		2133		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CK and CK#	C_{CK}	0.8	1.4	0.8	1.3	0.8	1.3	pF	
ΔC: CK to CK#	C_{DCK}	0	0.15	0	0.15	0	0.15	pF	
Single-end I/O : DQ, DM	C_{IO}	1.5	2.3	1.5	2.2	1.5	2.1	pF	2
Differential I/O : DQS, DQS#, TDQS, TDQS#	C_{IO}	1.5	2.3	1.5	2.2	1.5	2.1	pF	3
ΔC: DQS to DQS#,TDQS, TDQS#	C_{DDQS}	0	0.15	0	0.15	0	0.15	pF	3
ΔC: DQ to DQS	C_{DIO}	–0.5	0.3	–0.5	0.3	–0.5	0.3	pF	4
Inputs(CTRL, CMD, ADDR)	C_{I}	0.75	1.3	0.75	1.2	0.75	1.2	pF	5
ΔC: CTRL to CK	C_{DI_CTRL}	–0.4	0.2	–0.4	0.2	–0.4	0.2	pF	6
ΔC: CMD_ADDR to CK	$C_{DI\_CMD\_ADDR}$	–0.4	0.4	–0.4	0.4	–0.4	0.4	pF	7
ZQ pin capacitance	C_{ZQ}	–	3.0	–	3.0	–	3.0	pF	
Reset pin capacitance	C_{RE}	–	3.0	–	3.0	–	3.0	pF	

Note :
1. VDD = 1.5V ±0.075mV, VDDQ = VDD, VREF = VSS, *f* = 100 MHz, TC = 25°C. VOUT(DC) = 0.5 × VDDQ, VOUT = 0.1V (peak-to-peak).
2. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
3. Includes TDQS, TDQS#. CDDQS is for DQS vs. DQS# and TDQS vs. TDQS# separately.
4. CDIO = CIO(DQ) - 0.5 × (CIO(DQS) + CIO(DQS#)).
5. Excludes CK, CK#; CTRL = ODT, CS#, and CKE; CMD = RAS#, CAS#, and WE#; ADDR = A[*n*:0], BA[2:0].
6. CDI_CTRL = CI(CTRL) - 0.5 × (CCK(CK) + CCK(CK#)).
7. CDI_CMD_ADDR = CI(CMD_ADDR) - 0.5 × (CCK(CK) + CCK(CK#)).

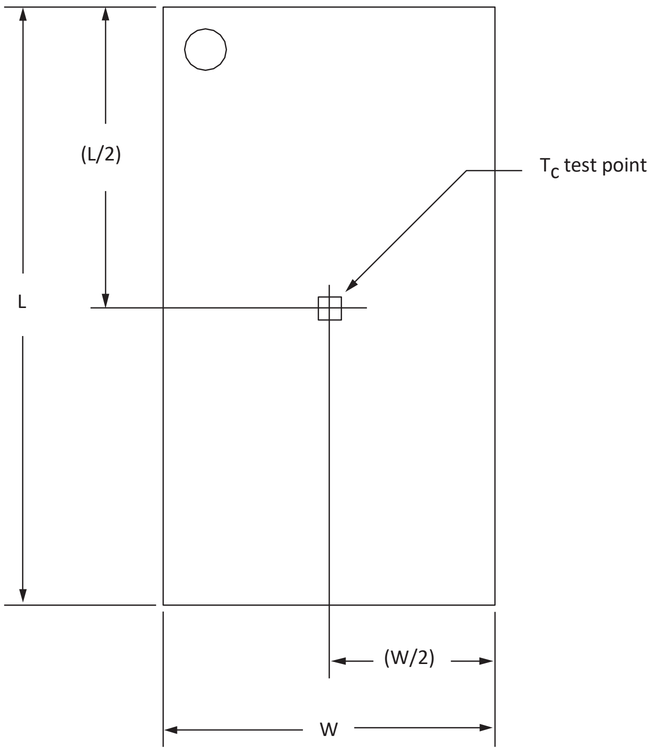
Thermal Characteristics

Table 3 : Thermal Characteristics

Parameter/Condition		Value	Units	Symbol	Notes
Operating case temperature – Commercial		0 to +85	°C	T_C	1, 2, 3
		0 to +95	°C	T_C	1, 2, 3, 4
Operating case temperature – Industrial		–40 to +85	°C	T_C	1, 2, 3
		–40 to +95	°C	T_C	1, 2, 3, 4
Operating case temperature – Automotive		–40 to +85	°C	T_C	1, 2, 3
		–40 to +105	°C	T_C	1, 2, 3, 4
Junction-to-case (TOP)	78-ball	-	°C/W	ΘJC	5
	96-ball	-			

Notes :
1. MAX operating case temperature. TC is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum TC during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum TC during operation.
4. If TC exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9µs interval refresh rate. The use of SRT or ASR must be enabled.
5. The thermal resistance data is based off of a number of samples from multiple lots and should be viewed as a typical number.

Figure 1 : Thermal Measurement Point



Electrical Specifications – IDD Specifications and Conditions

Within the following IDD measurement tables, the following definitions and conditions are used, unless stated otherwise :

- LOW: VIN ≤ VIL(AC)max; HIGH: VIN ≥ VIH(AC)min.
- Midlevel: Inputs are VREF = VDD/2.
- RON set to RZQ/7 (34Ω).
- $R_{TT,nom}$, set to RZQ/6 (40Ω).
- $R_{TT(WR)}$ set to RZQ/2 (120Ω).
- QOFF is enabled in MR1.
- ODT is enabled in MR1 ($R_{TT,nom}$) and MR2 ($R_{TT(WR)}$).
- TDQS is disabled in MR1.
- External DQ/DQS/DM load resistor is 25Ω to VDDQ/2.
- Burst lengths are BL8 fixed.
- AL equals 0 (except in IDD7).
- IDD specifications are tested after the device is properly initialized.
- Input slew rate is specified by AC parametric test conditions.
- ASR is disabled.
- Read burst type uses nibble sequential (MR0[3] = 0).
- Loop patterns must be executed at least once before current measurements begin.

Table 4: Timing Parameters Used for IDD Measurements – Clock Units

I_{DD} Parameter		DDR3 -800		DDR3 -1066		DDR3 -1333		DDR3 -1600		DDR3 -1866	DDR3 -2133	Unit
		5-5-5	6-6-6	7-7-7	8-8-8	9-9-9	10-10-10	10-10-10	11-11-11	13-13-13	14-14-14	
^{t}CK (MIN) I_{DD}		2.5		1.875		1.5		1.25		1.071	0.938	ns
CL I_{DD}		5	6	7	8	9	10	10	11	13	14	CK
^{t}RCD (MIN) I_{DD}		5	6	7	8	9	10	10	11	13	14	CK
^{t}RC (MIN) I_{DD}		20	21	27	28	33	34	38	39	45	50	CK
^{t}RAS (MIN) I_{DD}		15	15	20	20	24	24	28	28	32	36	CK
^{t}RP (MIN)		5	6	7	8	9	10	10	11	13	14	CK
^{t}FAW	x4, x8	16	16	20	20	20	20	24	24	26	27	CK
	x16	20	20	27	27	30	30	32	32	33	38	CK
^{t}RRD I_{DD}	x4, x8	4	4	4	4	4	4	5	5	5	6	CK
	x16	4	4	6	6	5	5	6	6	6	7	CK
^{t}RFC	1Gb	44	44	59	59	74	74	88	88	103	118	CK
	2Gb	64	64	86	86	107	107	128	128	150	172	CK
	4Gb	104	104	139	139	174	174	208	208	243	279	CK
	8Gb	140	140	187	187	234	234	280	280	328	375	CK

Table 5 : IDD0 Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
Toggling	Static HIGH	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D	1	0	0	0	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	0	0	0	0	0	0	0	–
			4	D#	1	1	1	1	0	0	0	0	0	0	0	–
				Repeat cycles 1 through 4 until *n*RAS - 1; truncate if needed												
			*n*RAS	PRE	0	0	1	0	0	0	0	0	0	0	0	–
				Repeat cycles 1 through 4 until *n*RC - 1; truncate if needed												
			*n*RC	ACT	0	0	1	1	0	0	0	0	0	F	0	–
			*n*RC + 1	D	1	0	0	0	0	0	0	0	0	F	0	–
			*n*RC + 2	D	1	0	0	0	0	0	0	0	0	F	0	–
			*n*RC + 3	D#	1	1	1	1	0	0	0	0	0	F	0	–
			*n*RC + 4	D#	1	1	1	1	0	0	0	0	0	F	0	–
				Repeat cycles *n*RC + 1 through *n*RC + 4 until *n*RC - 1 + *n*RAS -1; truncate if needed												
			*n*RC + *n*RAS	PRE	0	0	1	0	0	0	0	0	0	F	0	–
				Repeat cycles *n*RC + 1 through *n*RC + 4 until 2 × RC - 1; truncate if needed												
		1	2 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 1												
		2	4 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 2												
		3	6 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 3												
		4	8 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 4												
		5	10 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 5												
		6	12 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 6												
		7	14 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 7												

Note : 1. DQ, DQS, DQS# are midlevel.
2. DM is LOW.
3. Only selected bank (single) active.

Table 6 : IDD1 Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
Toggling	Static HIGH	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D	1	0	0	0	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	0	0	0	0	0	0	0	–
			4	D#	1	1	1	1	0	0	0	0	0	0	0	–
				Repeat cycles 1 through 4 until *n*RCD - 1; truncate if needed												
			*n*RCD	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
				Repeat cycles 1 through 4 until *n*RAS - 1; truncate if needed												
			*n*RAS	PRE	0	0	1	0	0	0	0	0	0	0	0	–
				Repeat cycles 1 through 4 until *n*RC - 1; truncate if needed												
			*n*RC	ACT	0	0	1	1	0	0	0	0	0	F	0	–
			*n*RC + 1	D	1	0	0	0	0	0	0	0	0	F	0	–
			*n*RC + 2	D	1	0	0	0	0	0	0	0	0	F	0	–
			*n*RC + 3	D#	1	1	1	1	0	0	0	0	0	F	0	–
			*n*RC + 4	D#	1	1	1	1	0	0	0	0	0	F	0	–
				Repeat cycles *n*RC + 1 through *n*RC + 4 until *n*RC + *n*RCD - 1; truncate if needed												
			*n*RC + *n*RCD	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
				Repeat cycles *n*RC + 1 through *n*RC + 4 until *n*RC + *n*RAS - 1; truncate if needed												
			*n*RC + *n*RAS	PRE	0	0	1	0	0	0	0	0	0	F	0	–
				Repeat cycle *n*RC + 1 through *n*RC + 4 until 2 × *n*RC - 1; truncate if needed												
		1	2 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 1												
		2	4 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 2												
		3	6 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 3												
		4	8 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 4												
		5	10 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 5												
		6	12 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 6												
		7	14 × *n*RC	Repeat sub-loop 0, use BA[2:0] = 7												

Notes :
1. DQ, DQS, DQS# are midlevel unless driven as required by the RD command.
2. DM is LOW.
3. Burst sequence is driven on each DQ signal by the RD command.
4. Only selected bank (single) active.

Table 7 : IDD Measurement Conditions for Power-Down Currents

Name	I_{DD2P0} Precharge Power-Down Current (Slow Exit)[1]	I_{DD2P1} Precharge Power-Down Current (Fast Exit)[1]	I_{DD2Q} Precharge Quiet Standby Current	I_{DD3P} Active Power-Down Current
Timing pattern	N/A	N/A	N/A	N/A
CKE	LOW	LOW	HIGH	LOW
External clock	Toggling	Toggling	Toggling	Toggling
^tCK	^tCK (MIN) I_{DD}	^tCK (MIN) I_{DD}	^tCK (MIN) I_{DD}	^tCK (MIN) I_{DD}
^tRC	N/A	N/A	N/A	N/A
^tRAS	N/A	N/A	N/A	N/A
^tRCD	N/A	N/A	N/A	N/A
^tRRD	N/A	N/A	N/A	N/A
^tRC	N/A	N/A	N/A	N/A
CL	N/A	N/A	N/A	N/A
AL	N/A	N/A	N/A	N/A
CS#	HIGH	HIGH	HIGH	HIGH
Command inputs	LOW	LOW	LOW	LOW
Row/column addr	LOW	LOW	LOW	LOW
Bank addresses	LOW	LOW	LOW	LOW
DM	LOW	LOW	LOW	LOW
Data I/O	Midlevel	Midlevel	Midlevel	Midlevel
Output buffer DQ, DQS	Enabled	Enabled	Enabled	Enabled
ODT[2]	Enabled, off	Enabled, off	Enabled, off	Enabled, off
Burst length	8	8	8	8
Active banks	None	None	None	All
Idle banks	All	All	All	None
Special notes	N/A	N/A	N/A	N/A

Notes :
1. MR0[12] defines DLL on/off behavior during precharge power-down only; DLL on (fast exit, MR0[12] = 1) and DLL off (slow exit, MR0[12] = 0).
2. “Enabled, off” means the MR bits are enabled, but the signal is LOW.

Table 8 : IDD2N and IDD3N Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
Toggling	Static HIGH	0	0	D	1	0	0	0	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D#	1	1	1	1	0	0	0	0	0	F	0	–
			3	D#	1	1	1	1	0	0	0	0	0	F	0	–
		1	4–7	Repeat sub-loop 0, use BA[2:0] = 1												
		2	8–11	Repeat sub-loop 0, use BA[2:0] = 2												
		3	12–15	Repeat sub-loop 0, use BA[2:0] = 3												
		4	16–19	Repeat sub-loop 0, use BA[2:0] = 4												
		5	20–23	Repeat sub-loop 0, use BA[2:0] = 5												
		6	24–27	Repeat sub-loop 0, use BA[2:0] = 6												
		7	28–31	Repeat sub-loop 0, use BA[2:0] = 7												

Notes :
1. DQ, DQS, DQS# are midlevel.
2. DM is LOW.
3. All banks closed during IDD2N; all banks open during IDD3N.

Table 9 : IDD2NT Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
Toggling	Static HIGH	0	0	D	1	0	0	0	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D#	1	1	1	1	0	0	0	0	0	F	0	–
			3	D#	1	1	1	1	0	0	0	0	0	F	0	–
		1	4–7	Repeat sub-loop 0, use BA[2:0] = 1; ODT = 0												
		2	8–11	Repeat sub-loop 0, use BA[2:0] = 2; ODT = 1												
		3	12–15	Repeat sub-loop 0, use BA[2:0] = 3; ODT = 1												
		4	16–19	Repeat sub-loop 0, use BA[2:0] = 4; ODT = 0												
		5	20–23	Repeat sub-loop 0, use BA[2:0] = 5; ODT = 0												
		6	24–27	Repeat sub-loop 0, use BA[2:0] = 6; ODT = 1												
		7	28–31	Repeat sub-loop 0, use BA[2:0] = 7; ODT = 1												

Notes :
1. DQ, DQS, DQS# are midlevel.
2. DM is LOW.
3. All banks closed.

Table 10 : IDD4R Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data^3
Toggling	Static HIGH	0	0	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D#	1	1	1	1	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	0	0	0	0	0	0	0	–
			4	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	0	0	0	F	0	–
			6	D#	1	1	1	1	0	0	0	0	0	F	0	–
			7	D#	1	1	1	1	0	0	0	0	0	F	0	–
		1	8–15	Repeat sub-loop 0, use BA[2:0] = 1												
		2	16–23	Repeat sub-loop 0, use BA[2:0] = 2												
		3	24–31	Repeat sub-loop 0, use BA[2:0] = 3												
		4	32–39	Repeat sub-loop 0, use BA[2:0] = 4												
		5	40–47	Repeat sub-loop 0, use BA[2:0] = 5												
		6	48–55	Repeat sub-loop 0, use BA[2:0] = 6												
		7	56–63	Repeat sub-loop 0, use BA[2:0] = 7												

Notes :
1. DQ, DQS, DQS# are midlevel when not driving in burst sequence.
2. DM is LOW.
3. Burst sequence is driven on each DQ signal by the RD command.
4. All banks open.

Table 11 : IDD4W Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static HIGH	0	0	WR	0	1	0	0	1	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	0	0	0	0	0	–
			2	D#	1	1	1	1	1	0	0	0	0	0	0	–
			3	D#	1	1	1	1	1	0	0	0	0	0	0	–
			4	WR	0	1	0	0	1	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	0	0	0	F	0	–
			6	D#	1	1	1	1	1	0	0	0	0	F	0	–
			7	D#	1	1	1	1	1	0	0	0	0	F	0	–
		1	8–15	Repeat sub-loop 0, use BA[2:0] = 1												
		2	16–23	Repeat sub-loop 0, use BA[2:0] = 2												
		3	24–31	Repeat sub-loop 0, use BA[2:0] = 3												
		4	32–39	Repeat sub-loop 0, use BA[2:0] = 4												
		5	40–47	Repeat sub-loop 0, use BA[2:0] = 5												
		6	48–55	Repeat sub-loop 0, use BA[2:0] = 6												
		7	56–63	Repeat sub-loop 0, use BA[2:0] = 7												

Notes :
1. DQ, DQS, DQS# are midlevel when not driving in burst sequence.
2. DM is LOW.
3. Burst sequence is driven on each DQ signal by the WR command.
4. All banks open.

Table 12 : IDD5B Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
Toggling	Static HIGH	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	–
		1a	1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D	1	0	0	0	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	0	0	0	0	0	F	0	–
			4	D#	1	1	1	1	0	0	0	0	0	F	0	–
		1b	5–8	Repeat sub-loop 1a, use BA[2:0] = 1												
		1c	9–12	Repeat sub-loop 1a, use BA[2:0] = 2												
		1d	13–16	Repeat sub-loop 1a, use BA[2:0] = 3												
		1e	17–20	Repeat sub-loop 1a, use BA[2:0] = 4												
		1f	21–24	Repeat sub-loop 1a, use BA[2:0] = 5												
		1g	25–28	Repeat sub-loop 1a, use BA[2:0] = 6												
		1h	29–32	Repeat sub-loop 1a, use BA[2:0] = 7												
		2	33–*n*RFC - 1	Repeat sub-loop 1a through 1h until *n*RFC - 1; truncate if needed												

Notes :
1. DQ, DQS, DQS# are midlevel.
2. DM is LOW.

Table 13 : IDD Measurement Conditions for IDD6, IDD6ET, and IDD8

I_{DD} Test	I_{DD6}: Self Refresh Current Normal Temperature Range T_C = 0°C to +85°C	I_{DD6ET}: Self Refresh Current Extended Temperature Range T_C = 0°C to +95°C	I_{DD8}: Reset[2]
CKE	LOW	LOW	Midlevel
External clock	Off, CK and CK# = LOW	Off, CK and CK# = LOW	Midlevel
^{t}CK	N/A	N/A	N/A
^{t}RC	N/A	N/A	N/A
^{t}RAS	N/A	N/A	N/A
^{t}RCD	N/A	N/A	N/A
^{t}RRD	N/A	N/A	N/A
^{t}RC	N/A	N/A	N/A
CL	N/A	N/A	N/A
AL	N/A	N/A	N/A
CS#	Midlevel	Midlevel	Midlevel
Command inputs	Midlevel	Midlevel	Midlevel
Row/column addresses	Midlevel	Midlevel	Midlevel
Bank addresses	Midlevel	Midlevel	Midlevel
Data I/O	Midlevel	Midlevel	Midlevel
Output buffer DQ, DQS	Enabled	Enabled	Midlevel
ODT[1]	Enabled, midlevel	Enabled, midlevel	Midlevel
Burst length	N/A	N/A	N/A
Active banks	N/A	N/A	None
Idle banks	N/A	N/A	All
SRT	Disabled (normal)	Enabled (extended)	N/A
ASR	Disabled	Disabled	N/A

Notes :
1. "Enabled, midlevel" means the MR command is enabled, but the signal is midlevel.
2. During a cold boot RESET (initialization), current reading is valid after power is stable and RESET has been LOW for 1ms; During a warm boot RESET (while operating), current reading is valid after RESET has been LOW for 200ns + tRFC.

Table 14 : IDD7 Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static HIGH	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	–
			1	RDA	0	1	0	1	0	0	0	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	0	0	0	0	0	–
			3	Repeat cycle 2 until *n*RRD - 1												
		1	*n*RRD	ACT	0	0	1	1	0	1	0	0	0	F	0	–
			*n*RRD + 1	RDA	0	1	0	1	0	1	0	1	0	F	0	00110011
			*n*RRD + 2	D	1	0	0	0	0	1	0	0	0	F	0	–
			*n*RRD + 3	Repeat cycle *n*RRD + 2 until 2 × *n*RRD - 1												
		2	2 × *n*RRD	Repeat sub-loop 0, use BA[2:0] = 2												
		3	3 × *n*RRD	Repeat sub-loop 1, use BA[2:0] = 3												
		4	4 × *n*RRD	D	1	0	0	0	0	3	0	0	0	F	0	–
			4 × *n*RRD + 1	Repeat cycle 4 × *n*RRD until *n*FAW - 1, if needed												
		5	*n*FAW	Repeat sub-loop 0, use BA[2:0] = 4												
		6	*n*FAW + *n*RRD	Repeat sub-loop 1, use BA[2:0] = 5												
		7	*n*FAW + 2 × *n*RRD	Repeat sub-loop 0, use BA[2:0] = 6												
		8	*n*FAW + 3 × *n*RRD	Repeat sub-loop 1, use BA[2:0] = 7												
		9	*n*FAW + 4 × *n*RRD	D	1	0	0	0	0	7	0	0	0	F	0	–
			*n*FAW + 4 × *n*RRD + 1	Repeat cycle *n*FAW + 4 × *n*RRD until 2 × *n*FAW - 1, if needed												
		10	2 × *n*FAW	ACT	0	0	1	1	0	0	0	0	0	F	0	–
			2 × *n*FAW + 1	RDA	0	1	0	1	0	0	0	1	0	F	0	00110011
			2 × *n*FAW + 2	D	1	0	0	0	0	0	0	0	0	F	0	–
			2 × *n*FAW + 3	Repeat cycle 2 × *n*FAW + 2 until 2 × *n*FAW + *n*RRD - 1												
		11	2 × *n*FAW + *n*RRD	ACT	0	0	1	1	0	1	0	0	0	0	0	–
			2 × *n*FAW + *n*RRD + 1	RDA	0	1	0	1	0	1	0	1	0	0	0	00000000
			2 × *n*FAW + *n*RRD + 2	D	1	0	0	0	0	1	0	0	0	0	0	–
			2 × *n*FAW + *n*RRD + 3	Repeat cycle 2 × *n*FAW + *n*RRD + 2 until 2 × *n*FAW + 2 × *n*RRD - 1												
		12	2 × *n*FAW + 2 × *n*RRD	Repeat sub-loop 10, use BA[2:0] = 2												
		13	2 × *n*FAW + 3 × *n*RRD	Repeat sub-loop 11, use BA[2:0] = 3												
		14	2 × *n*FAW + 4 × *n*RRD	D	1	0	0	0	0	3	0	0	0	0	0	–
			2 × *n*FAW + 4 × *n*RRD + 1	Repeat cycle 2 × *n*FAW + 4 × *n*RRD until 3 × *n*FAW - 1, if needed												
		15	3 × *n*FAW	Repeat sub-loop 10, use BA[2:0] = 4												
		16	3 × *n*FAW + *n*RRD	Repeat sub-loop 11, use BA[2:0] = 5												
		17	3 × *n*FAW + 2 × *n*RRD	Repeat sub-loop 10, use BA[2:0] = 6												
		18	3 × *n*FAW + 3 × *n*RRD	Repeat sub-loop 11, use BA[2:0] = 7												
		19	3 × *n*FAW + 4 × *n*RRD	D	1	0	0	0	0	7	0	0	0	0	0	–
			3 × *n*FAW + 4 × *n*RRD + 1	Repeat cycle 3 × *n*FAW + 4 × *n*RRD until 4 × *n*FAW - 1, if needed												

Notes : 1. DQ, DQS, DQS# are midlevel unless driven as required by the RD command.
2. DM is LOW.
3. Burst sequence is driven on each DQ signal by the RD command.
4. AL = CL-1.

Electrical Characteristics – IDD Specifications

Table 15 : IDD Maximum Limits

Speed Bin			DDR3 -1600	DDR3 -1866	DDR3 -2133	Units	Notes
Parameter	**Symbol**	**Width**					
Operating current 0: One bank ACTIVATE-to-RECHARGE	IDD0	X4, X8	95	105	110	mA	1, 2
		X16	115	120	130	mA	1, 2
Operating current 1: One bank ACTIVATE-to-READ to- PRECHARGE	IDD1	X4, X8	110	115	120	mA	1, 2
		X16	125	130	135	mA	1, 2
Precharge power-down current; Slow exit	IDD2PD (slow)	All	14	14	14	mA	1, 2
Precharge power-down current; Fast exit	IDD2P1 (fast)	All	35	40	45	mA	1, 2
Precharge quiet standby Current	IDD2Q	All	65	70	75	mA	1, 2
Precharge standby current	IDD2N	All	70	75	80	mA	1, 2
Precharge standby ODT current	IDD2NT	X4, X8	68	75	85	mA	1, 2
		X16	70	80	90	mA	1, 2
Active power-down current	IDD3P	X4, X8	50	60	65	mA	1, 2
		X16	60	70	75	mA	1, 2
Active standby current	IDD3N	X4, X8	100	110	120	mA	1, 2
		X16	130	150	160	mA	1, 2
Burst read operating current	IDD4R	X4, X8	145	160	175	mA	1, 2
		X16	200	220	240	mA	1, 2
Burst write operating current	IDD4W	X4, X8	160	175	190	mA	1, 2
		X16	240	260	280	mA	1, 2
Burst refresh current	IDD5B	X4, X8	145	150	160	mA	1, 2
		X16	150	155	165	mA	1, 2
Room temperature self refresh	IDD6	All	11	11	11	mA	1, 2, 3
Extended temperature self refresh	IDD6ET	All	12	12	12	mA	1, 4
All banks interleaved read current	IDD7	X4, X8	155	165	190	mA	1, 2
		X16	210	220	240	mA	1, 2
Reset current	IDD8	All	11	11	11	mA	1, 2

Notes :
1. TC = 85°C; SRT and ASR are disabled.
2. Enabling ASR could increase IDD*x* by up to an additional 2mA.
3. Restricted to TC (MAX) = 85°C.
4. TC = 85°C; ASR and ODT are disabled; SRT is enabled.
5. The IDD values must be derated (increased) on IT-option and AT-option devices when operated outside of the range 0°C ≤ TC ≤ +85°C:
   5a. When TC < 0°C: IDD2P0, IDD2P1 and IDD3P must be derated by 4%; IDD4R and IDD4W must be derated by 2%; and IDD6 and IDD7 must be derated by 7%.
   5b. When TC > 85°C: IDD0, IDD1, IDD2N, IDD2NT, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, and IDD5B must be derated by 2%; IDD2Px must be derated by 30%.

Electrical Specifications – DC and AC

DC Operating Conditions

Table 16 : DC Electrical Characteristics and Operating Conditions

All voltages are referenced to VSS

Parameter/Condition	Symbol	Min	Nom	Max	Unit	Notes
Supply voltage	V_{DD}	1.425	1.5	1.575	V	1, 2
I/O supply voltage	V_{DDQ}	1.425	1.5	1.575	V	1, 2
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.1V (All other pins not under test = 0V)	I_I	–2	–	2	µA	
V_{REF} supply leakage current $V_{REFDQ} = V_{DD}/2$ or $V_{REFCA} = V_{DD}/2$ (All other pins not under test = 0V)	I_{VREF}	–1	–	1	µA	3, 4

Notes :
1. VDD and VDDQ must track one another. VDDQ must be ≤ VDD. VSS = VSSQ.
2. VDD and VDDQ may include AC noise of ±50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. VDD and VDDQ must be at same level for valid AC timing parameters.
3. VREF (see Table 17).
4. The minimum limit requirement is for testing purposes. The leakage current on the VREF pin should be minimal.

Input Operating Conditions

Table 17 : DC Electrical Characteristics and Input Conditions

All voltages are referenced to VSS

Parameter/Condition	Symbol	Min	Nom	Max	Unit	Notes
V_{IN} low; DC/commands/address busses	V_{IL}	V_{SS}	N/A	See Table 18	V	
V_{IN} high; DC/commands/address busses	V_{IH}	See Table 18	N/A	V_{DD}	V	
Input reference voltage command/address bus	$V_{REFCA(DC)}$	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	1, 2
I/O reference voltage DQ bus	$V_{REFDQ(DC)}$	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	2, 3
I/O reference voltage DQ bus in SELF REFRESH	$V_{REFDQ(SR)}$	V_{SS}	$0.5 \times V_{DD}$	V_{DD}	V	4
Command/address termination voltage (system level, not direct DRAM input)	V_{TT}	–	$0.5 \times V_{DDQ}$	–	V	5

Notes :
1. VREFCA(DC) is expected to be approximately 0.5 × VDD and to track variations in the DC level. Externally generated peak noise (noncommon mode) on VREFCA may not exceed ±1%×VDD around the VREFCA(DC) value. Peak-to-peak AC noise on VREFCA should not exceed ±2% of VREFCA(DC).
2. DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.
3. VREFDQ(DC) is expected to be approximately 0.5 × VDD and to track variations in the DC level. Externally generated peak noise (noncommon mode) on VREFDQ may not exceed ±1%×VDD around the VREFDQ(DC) value. Peak-to-peak AC noise on VREFDQ should not exceed ±2% of VREFDQ(DC).

Table 18 : Input Switching Conditions

Parameter/Condition	Symbol	DDR3-800 DDR3-1066	DDR3-1333 DDR3-1600	DDR3-1866 DDR3-2133	Unit
Command and Address					
Input high AC voltage: Logic 1 @ 175mV	$V_{IH(AC175)min}$	175	175	–	mV
Input high AC voltage: Logic 1 @ 150mV	$V_{IH(AC150)min}$	150	150	–	mV
Input high AC voltage: Logic 1 @ 135 mV	$V_{IH(AC135)min}$	–	–	135	mV
Input high AC voltage: Logic 1 @ 125 mV	$V_{IH(AC125)min}$	–	–	125	mV
Input high DC voltage: Logic 1 @ 100 mV	$V_{IH(DC100)min}$	100	100	100	mV
Input low DC voltage: Logic 0 @ –100mV	$V_{IL(DC100)max}$	–100	–100	–100	mV
Input low AC voltage: Logic 0 @ –125mV	$V_{IL(AC125)max}$	–	–	–125	mV
Input low AC voltage: Logic 0 @ –135mV	$V_{IL(AC135)max}$	–	–	–135	mV
Input low AC voltage: Logic 0 @ –150mV	$V_{IL(AC150)max}$	–150	–150	–	mV
Input low AC voltage: Logic 0 @ –175mV	$V_{IL(AC175)max}$	–175	–175	–	mV
DQ and DM					
Input high AC voltage: Logic 1	$V_{IH(AC175)min}$	175	–	–	mV
Input high AC voltage: Logic 1	$V_{IH(AC150)min}$	150	150	–	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}$	–	–	135	mV
Input high DC voltage: Logic 1	$V_{IH(DC100)min}$	100	100	100	mV
Input low DC voltage: Logic 0	$V_{IL(DC100)max}$	–100	–100	–100	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)max}$	–	–	–135	mV
Input low AC voltage: Logic 0	$V_{IL(AC150)max}$	–150	–150	–	mV
Input low AC voltage: Logic 0	$V_{IL(AC175)max}$	–175	–	–	mV

Notes :

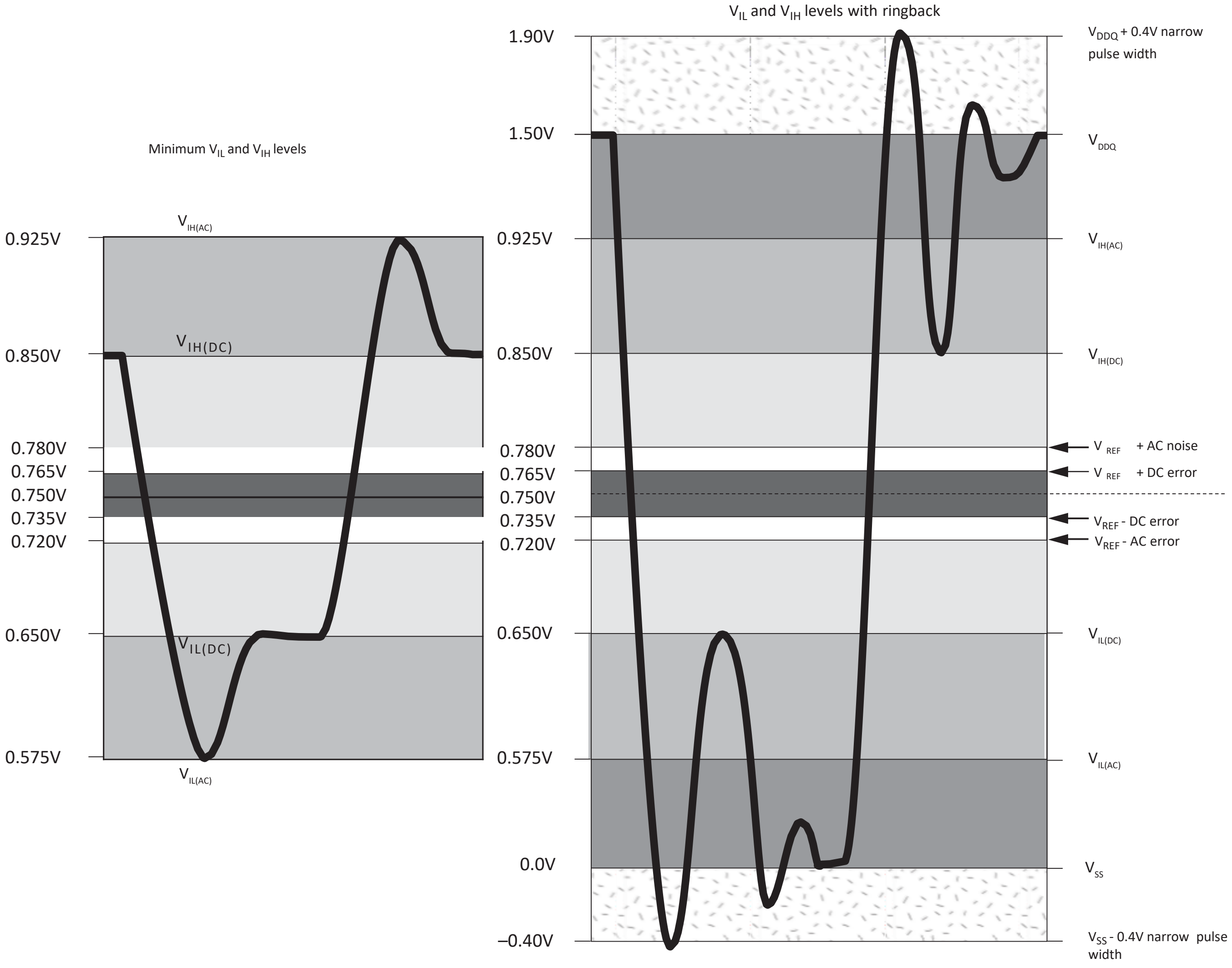
1. All voltages are referenced to VREF. VREF is VREFCA for control, command, and address. All slew rates and setup/ hold times are specified at the DRAM ball. VREF is VREFDQ for DQ and DM inputs.
2. Input setup timing parameters (tIS and tDS) are referenced at VIL(AC)/VIH(AC), not VREF(DC).
3. Input hold timing parameters (tIH and tDH) are referenced at VIL(DC)/VIH(DC), not VREF(DC).
4. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).
5. When two VIH(AC) values (and two corresponding VIL(AC) values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used.
   Additionally, one VIH(AC) value may be used for address/command inputs and the other VIH(AC) value may be used for data inputs. For example, for DDR3-800, two input AC levels are defined : VIH(AC175),min and VIH(AC150), min(corresponding VIL(AC175),min and VIL(AC150),min). For DDR3-800, the address / command inputs must use either VIH(AC175),min with tIS(AC175) of 200ps or VIH(AC150),min with tIS(AC150) of 350ps; independently, the data inputs must use either VIH(AC175),min with tDS(AC175) of 75ps or VIH(AC150),min with tDS(AC150) of 125ps.

Table 19 : Differential Input Operating Conditions (CK, CK# and DQS, DQS#)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Differential input voltage logic high - slew	$V_{IH,diff}$	200	N/A	mV	4
Differential input voltage logic low - slew	$V_{IL,diff}$	N/A	–200	mV	4
Differential input voltage logic high	$V_{IH,diff(AC)}$	2 × ($V_{IH(AC)}$ - V_{REF})	V_{DD}/V_{DDQ}	mV	5
Differential input voltage logic low	$V_{IL,diff(AC)}$	V_{SS}/V_{SSQ}	2 × ($V_{IL(AC)}$-V_{REF})	mV	6
Differential input crossing voltage relative to $V_{DD}/2$ for DQS, DQS#; CK, CK#	V_{IX}	$V_{REF(DC)}$ - 150	$V_{REF(DC)}$ + 150	mV	4, 7
Differential input crossing voltage relative to $V_{DD}/2$ for CK, CK#	V_{IX} (175)	$V_{REF(DC)}$ - 175	$V_{REF(DC)}$ + 175	mV	4, 7, 8
Single-ended high level for strobes	V_{SEH}	$V_{DDQ}/2$ + 175	V_{DDQ}	mV	5
Single-ended high level for CK, CK#		$V_{DD}/2$ + 175	V_{DD}	mV	5
Single-ended low level for strobes	V_{SEL}	V_{SSQ}	$V_{DDQ}/2$ - 175	mV	6
Single-ended low level for CK, CK#		V_{SS}	$V_{DD}/2$ - 175	mV	6

Notes :
1. Clock is referenced to VDD and VSS. Data strobe is referenced to VDDQ and VSSQ.
2. Reference is VREFCA(DC) for clock and VREFDQ(DC) for strobe.
3. Differential input slew rate = 2 V/ns
4. Defines slew rate reference points, relative to input crossing voltages.
5. Minimum DC limit is relative to single-ended signals; overshoot specifications are applicable.
6. Maximum DC limit is relative to single-ended signals; undershoot specifications are applicable.
7. The typical value of VIX(AC) is expected to be about 0.5 × VDD of the transmitting device, and VIX(AC) is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input signals must cross.
8. The VIX extended range (±175mV) is allowed only for the clock; this VIX extended range is only allowed when the following conditions are met: The single-ended input signals are monotonic, have the single-ended swing VSEL, VSEH of at least VDD/2 ±250mV, and the differential slew rate of CK, CK# is greater than 3 V/ns.
9. VIX must provide 25mV (single-ended) of the voltages separation.

Figure 2 : Input Signal



Notes : 1. Numbers in diagrams reflect nominal values.

AC Overshoot/Undershoot Specification

Table 20 : Control and Address Pins

Parameter	DDR3 -800	DDR3 -1066	DDR3 -1333	DDR3 -1600	DDR3 -1866	DDR3 -2133
Maximum peak amplitude allowed for overshoot area (see Figure 3)	0.4V	0.4V	0.4V	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure 4)	0.4V	0.4V	0.4V	0.4V	0.4V	0.4V
Maximum overshoot area above V_{DD} (see Figure 3)	0.67 Vns	0.5 Vns	0.4 Vns	0.33 Vns	0.28 Vns	0.25 Vns
Maximum undershoot area below V_{SS} (see Figure 4)	0.67 Vns	0.5 Vns	0.4 Vns	0.33 Vns	0.28 Vns	0.25 Vns

Table 21 : Clock, Data, Strobe, and Mask Pins

Parameter	DDR3 -800	DDR3 -1066	DDR3 -1333	DDR3 -1600	DDR3 -1866	DDR3 -2133
Maximum peak amplitude allowed for overshoot area (see Figure 3)	0.4V	0.4V	0.4V	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure 4)	0.4V	0.4V	0.4V	0.4V	0.4V	0.4V
Maximum overshoot area above V_{DD}/V_{DDQ} (see Figure 3)	0.25 Vns	0.19 Vns	0.15 Vns	0.13 Vns	0.11 Vns	0.10 Vns
Maximum undershoot area below V_{SS}/V_{SSQ} (see Figure 4)	0.25 Vns	0.19 Vns	0.15 Vns	0.13 Vns	0.11 Vns	0.10 Vns

Figure 3 : Overshoot

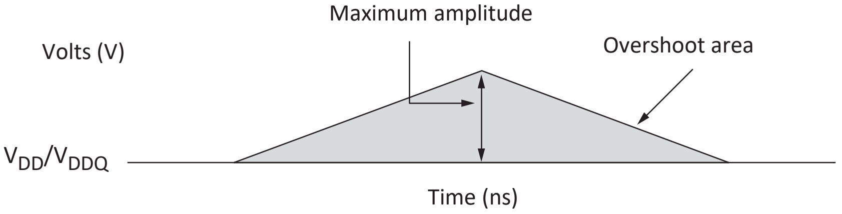


Figure 4 : Undershoot

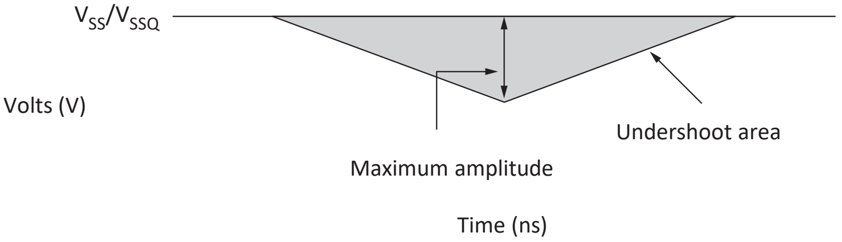


Figure 5 : VIX for Differential Signals

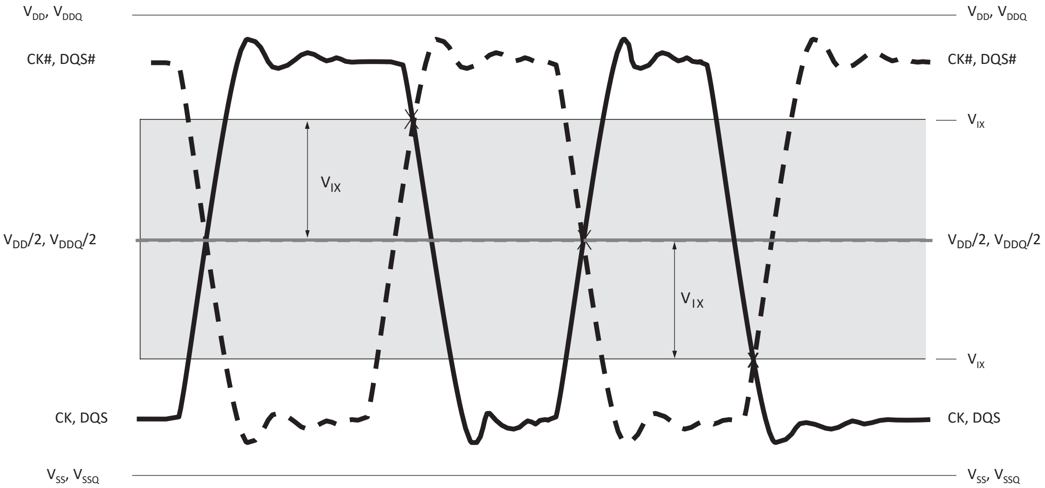


Figure 6 : Single-Ended Requirements for Differential Signals

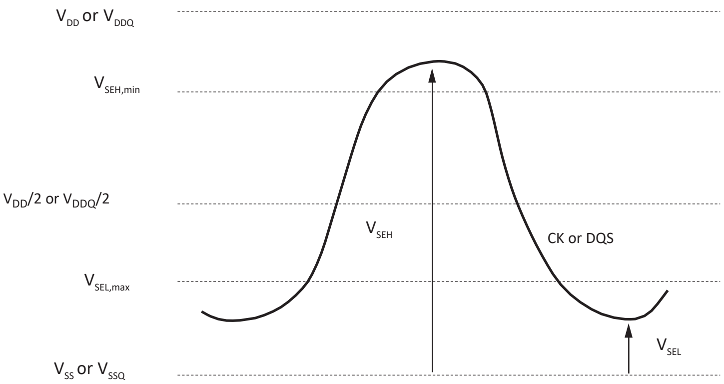


Figure 7 : Definition of Differential AC-Swing and tDVAC

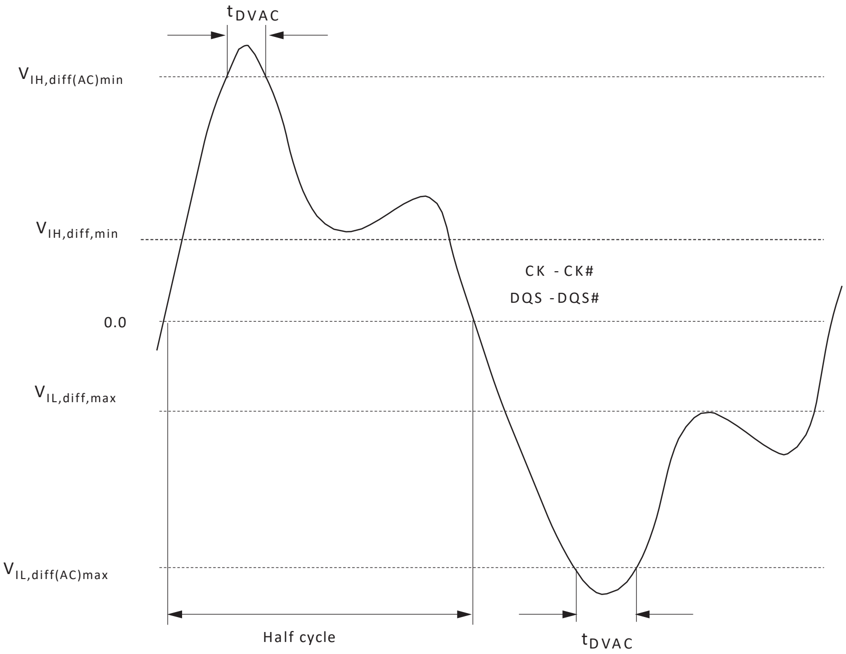


Table 22 : Allowed Time Before Ringback (tDVAC) for CK - CK# and DQS - DQS#

Slew Rate (V/ns)	^{t}DVAC (ps) at $\lvert V_{IH,diff(AC)}$ to $V_{IL,diff(AC)} \rvert$	
	350mV	300mV
>4.0	75	175
4.0	57	170
3.0	50	167
2.0	38	163
1.9	34	162
1.6	29	161
1.4	22	159
1.2	13	155
1.0	0	150
<1.0	0	150

Note: 1. Below VIL(AC)

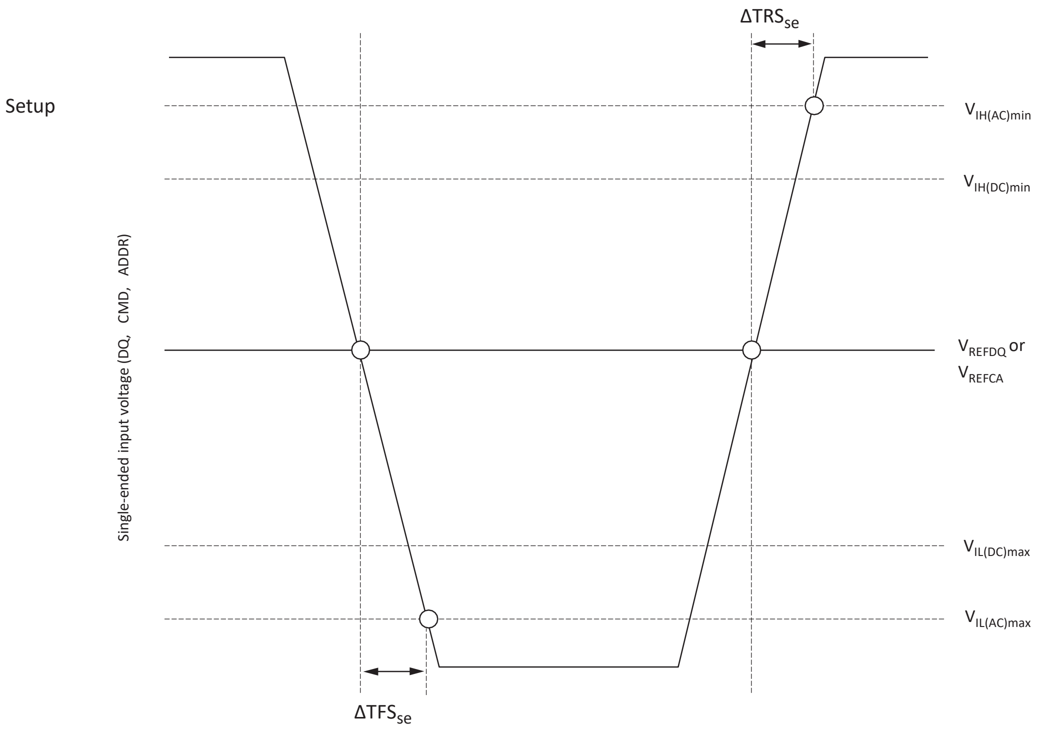
Slew Rate Definitions for Single-Ended Input Signals

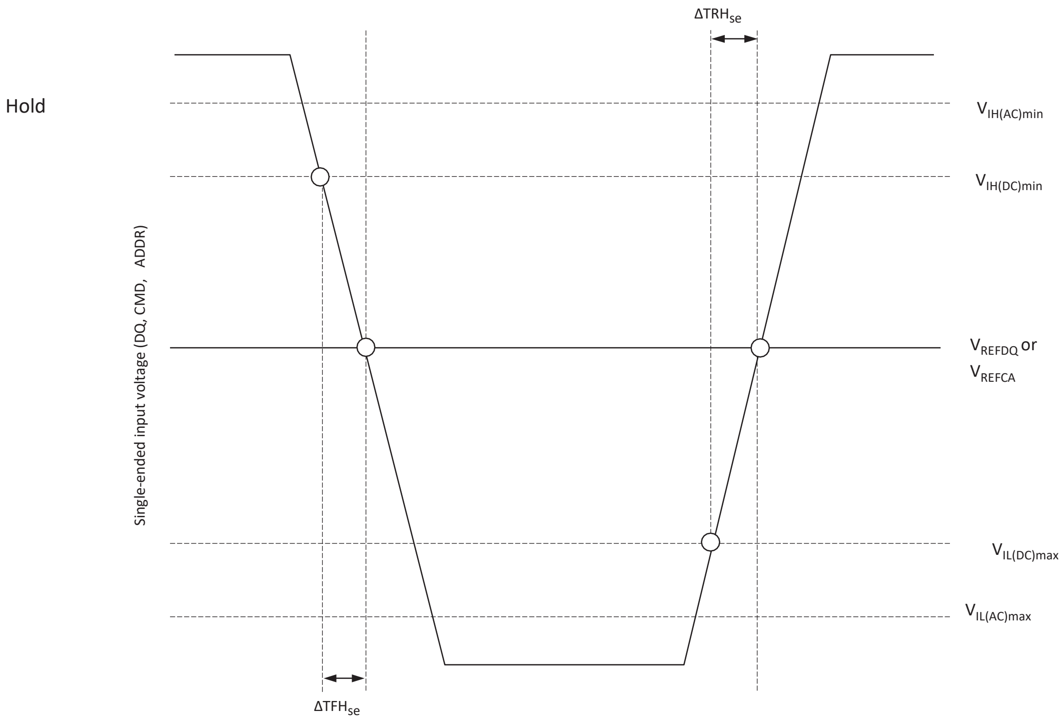
Setup (tIS and tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF and the first crossing of VIH(AC)min. Setup (tIS and tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF and the first crossing of VIL(AC)max. Hold (tIH and tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VREF. Hold (tIH and tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VREF.

Table 23 : Single-Ended Input Slew Rate Definition

Input Slew Rates (Linear Signals)		Measured		Calculation
Input	**Edge**	**From**	**To**	
Setup	Rising	V_{REF}	$V_{IH(AC)min}$	$\frac{V_{IH(AC),min} - V_{REF}}{\Delta TRS_{se}}$
	Falling	V_{REF}	$V_{IL(AC)max}$	$\frac{V_{REF} - V_{IL(AC),max}}{\Delta TFS_{se}}$
Hold	Rising	$V_{IL(DC)max}$	V_{REF}	$\frac{V_{REF} - V_{IL(DC),max}}{\Delta TFH_{se}}$
	Falling	$V_{IH(DC)min}$	V_{REF}	$\frac{V_{IH(DC),min} - V_{REF}}{\Delta TRSH_{se}}$

Figure 8 : Nominal Slew Rate Definition for Single-Ended Input Signals





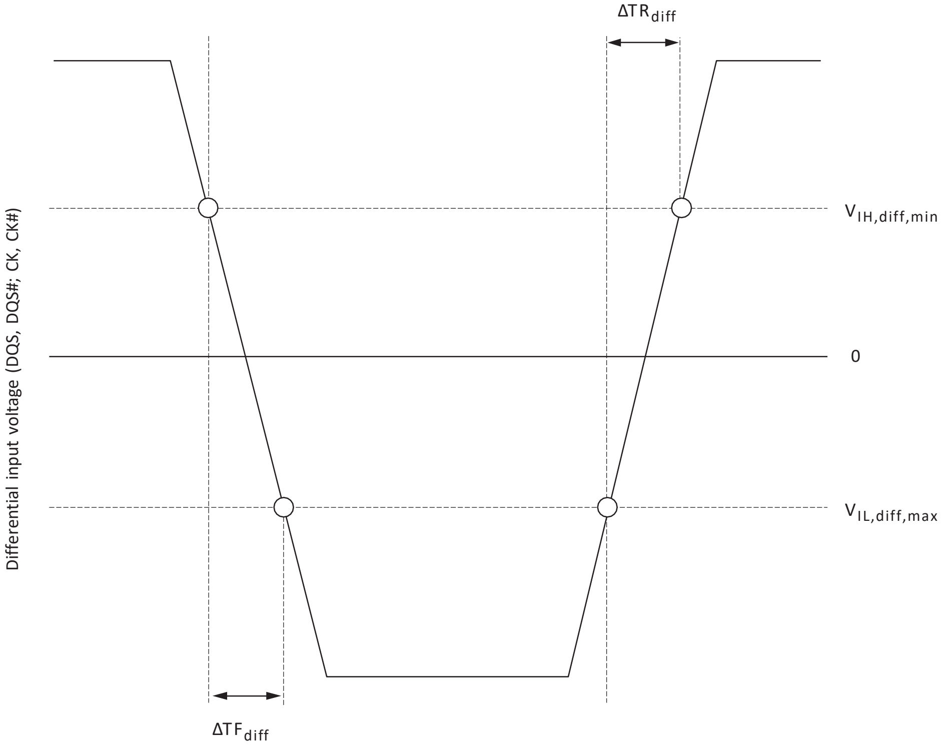
Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured. The nominal slew rate for a rising signal is defined as the slew rate between VIL,diff,max and VIH,diff,min. The nominal slew rate for a falling signal is defined as the slew rate between VIH, diff,min and VIL, diff,max.

Table 24 : Differential Input Slew Rate Definition

Differential Input Slew Rates (Linear Signals)		Measured		Calculation
Input	**Edge**	**From**	**To**	
CK and DQS reference	Rising	$V_{IL,diff,max}$	$V_{IH,diff,min}$	$\frac{V_{IH,diff,min} - V_{IL,diff,max}}{\Delta TR_{diff}}$
	Falling	$V_{IH,diff,min}$	$V_{IL,diff,max}$	$\frac{V_{IH,diff,min} - V_{IL,diff,max}}{\Delta TF_{diff}}$

Figure 9: Nominal Differential Input Slew Rate Definition for DQS, DQS# and CK, CK#



ODT Characteristics

The ODT effective resistance R_{TT} is defined by MR1[9, 6, and 2]. ODT is applied to the DQ, DM, DQS, DQS#, and TDQS, TDQS# balls (x8 devices only). The ODT target values and a functional representation are listed in Table 25 and Table 26 .

The individual pull-up and pull-down resistors ($R_{TT(PU)}$) and ($R_{TT(PD)}$) are defined as follows:

- $R_{TT(PU)}$ = (VDDQ - VOUT)/|IOUT|, under the condition that $R_{TT(PD)}$ is turned off
- $R_{TT(PD)}$ = (VOUT)/|IOUT|, under the condition that $R_{TT(PU)}$ is turned off

Figure 10 : ODT Levels and I-V Characteristics

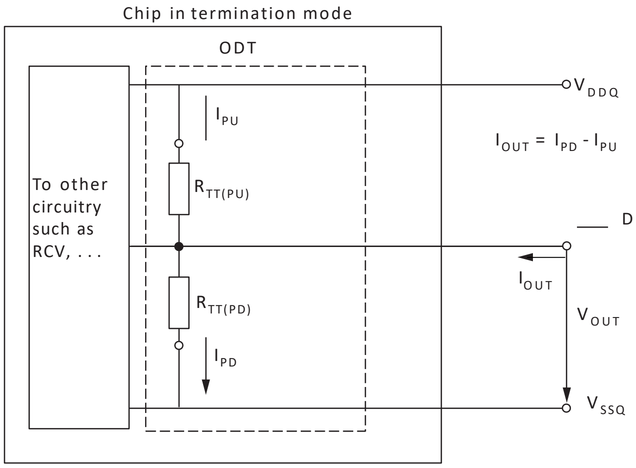


Table 25 : On-Die Termination DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Nom	Max	Unit	Notes
R_{TT} effective impedance	$R_{TT(EFF)}$	See Table 26				1, 2
Deviation of VM with respect to $V_{DDQ}/2$	ΔVM	–5		5	%	1, 2, 3

Notes :
1. Tolerance limits are applicable after proper ZQ calibration has been performed at a stable temperature and voltage (VDDQ = VDD, VSSQ = VSS). Refer to ODT Sensitivity if either the temperature or voltage changes after calibration.
2. Measurement definition for R_{TT} : Apply VIH(AC) to pin under test and measure current I[VIH(AC)], then apply VIL(AC) to pin under test and measure current I[VIL(AC)] : R_{TT} = (VIH(AC) - VIL(AC)) /(I(VIH(AC)) - I(VIL(AC))
3. Measure voltage (VM) at the tested pin with no load : ΔVM = 2 × VM – 1 VDDQ × 100
4. For IT and AT devices, the minimum values are derated by 6% when the device operates between –40°C and 0°C (TC).

ODT Resistors

Table 26 provides an overview of the ODT DC electrical characteristics. The values provided are not specification requirements; however, they can be used as design guidelines to indicate what R_{TT} is targeted to provide:

- R_{TT} 120Ω is made up of $R_{TT120(PD240)}$ and $R_{TT120(PU240)}$
- R_{TT} 60Ω is made up of $R_{TT60(PD120)}$ and $R_{TT60(PU120)}$
- R_{TT} 40Ω is made up of $R_{TT40(PD80)}$ and $R_{TT40(PU80)}$
- R_{TT} 30Ω is made up of $R_{TT30(PD60)}$ and $R_{TT30(PU60)}$
- R_{TT} 20Ω is made up of $R_{TT20(PD40)}$ and $R_{TT20(PU40)}$

Table 26 : R_{TT} Effective Impedances

MR1 [9, 6, 2]	R_{TT}	Resistor	V_{OUT}	Min	Nom	Max	Unit
0, 1, 0	120Ω	$R_{TT120(PD240)}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/1
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/1
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/1
		$R_{TT120(PU240)}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/1
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/1
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/1
	120Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/2
0, 0, 1	60Ω	$R_{TT60(PD120)}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/2
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/2
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/2
		$R_{TT60(PU120)}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/2
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/2
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/2
	60Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/4
0, 1, 1	40Ω	$R_{TT40(PD80)}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/3
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/3
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/3
		$R_{TT40(PU80)}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/3
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/3
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/3
	40Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/6
1, 0, 1	30Ω	$R_{TT30(PD60)}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/4
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/4
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/4
		$R_{TT30(PU60)}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/4
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/4
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/4
	30Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/8

Table 26 : RTT Effective Impedances (Continued)

MR1 [9, 6, 2]	R_{TT}	Resistor	V_{OUT}	Min	Nom	Max	Unit
1, 0, 0	20Ω	$R_{TT20(PD40)}$	$0.2 \times V_{DDQ}$	0.6	1.0	1.1	RZQ/6
			$0.5 \times V_{DDQ}$	0.9	1.0	1.1	RZQ/6
			$0.8 \times V_{DDQ}$	0.9	1.0	1.4	RZQ/6
		$R_{TT20(PU40)}$	$0.2 \times V_{DDQ}$	0.9	1.0	1.4	RZQ/6
			$0.5 \times V_{DDQ}$	0.9	1.0	1.1	RZQ/6
			$0.8 \times V_{DDQ}$	0.6	1.0	1.1	RZQ/6
	20Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/12

Note: 1. Values assume an RZQ of 240Ω(   ).

ODT Sensitivity

If either the temperature or voltage changes after I/O calibration, then the tolerance limits listed in Table 25 and Table 26 can be expected to widen according to Table 27 and Table 28.

Table 27 : ODT Sensitivity Definition

Symbol	Min	Max	Unit
R_{TT}	$0.9 - dR_{TT}dT \times \lvert DT \rvert - dR_{TT}dV \times \lvert DV \rvert$	$1.6 + dR_{TT}dT \times \lvert DT \rvert + dR_{TT}dV \times \lvert DV \rvert$	RZQ/(2, 4, 6, 8, 12)

Note: 1. ΔT = T - T(@ calibration), ΔV = VDDQ - VDDQ(@ calibration) and VDD = VDDQ.

Table 28 : ODT Temperature and Voltage Sensitivity

Change	Min	Max	Unit
$dR_{TT}dT$	0	1.5	%/°C
$dR_{TT}dV$	0	0.15	%/mV

ODT Timing Definitions

ODT loading differs from that used in AC timing measurements. The reference load for ODT timings is shown in Figure 11. Two parameters define when ODT turns on or off synchronously, two define when ODT turns on or off asynchronously, and another defines when ODT turns on or off dynamically. Table 29 outlines and provides definition and measurement references settings for each parameter(see Table 30)

ODT turn-on time begins when the output leaves High-Z and ODT resistance begins to turn on. ODT turn-off time begins when the output leaves Low-Z and ODT resistance begins to turn off.

Figure 11: ODT Timing Reference Load

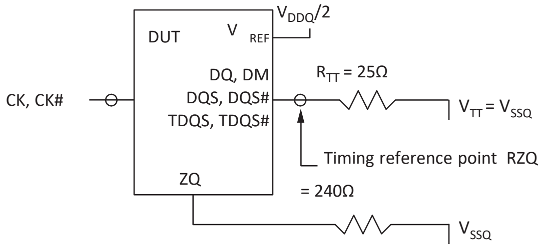


Table 29 : ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure
^tAON	Rising edge of CK - CK# defined by the end point of ODTLon	Extrapolated point at V_{SSQ}	Figure 12
^tAOF	Rising edge of CK - CK# defined by the end point of ODTLoff	Extrapolated point at $V_{RTT,nom}$	Figure 12
^tAONPD	Rising edge of CK - CK# with ODT first being registered HIGH	Extrapolated point at V_{SSQ}	Figure 13
^tAOFPD	Rising edge of CK - CK# with ODT first being registered LOW	Extrapolated point at $V_{RTT,nom}$	Figure 13
^tADC	Rising edge of CK - CK# defined by the end point of ODTLcnw, ODTLcwn4, or ODTLcwn8	Extrapolated points at $V_{RTT(WR)}$ and $V_{RTT,nom}$	Figure 14

Table 30: Reference Settings for ODT Timing Measurements

Measured Parameter	$R_{TT,nom}$ Setting	$R_{TT(WR)}$ Setting	V_{SW1}	V_{SW2}
^tAON	RZQ/4 (60Ω)	N/A	50mV	100mV
	RZQ/12 (20Ω)	N/A	100mV	200mV
^tAOF	RZQ/4 (60Ω)	N/A	50mV	100mV
	RZQ/12 (20Ω)	N/A	100mV	200mV
^tAONPD	RZQ/4 (60Ω)	N/A	50mV	100mV
	RZQ/12 (20Ω)	N/A	100mV	200mV
^tAOFPD	RZQ/4 (60Ω)	N/A	50mV	100mV
	RZQ/12 (20Ω)	N/A	100mV	200mV
^tADC	RZQ/12 (20Ω)	RZQ/2 (120Ω)	200mV	300mV

Note: 1. Assume an RZQ of 240Ω (±1%) and that proper ZQ calibration has been performed at a stable temperature and voltage (VDDQ = VDD, VSSQ = VSS).

Figure 12 : tAON and tAOF Definitions

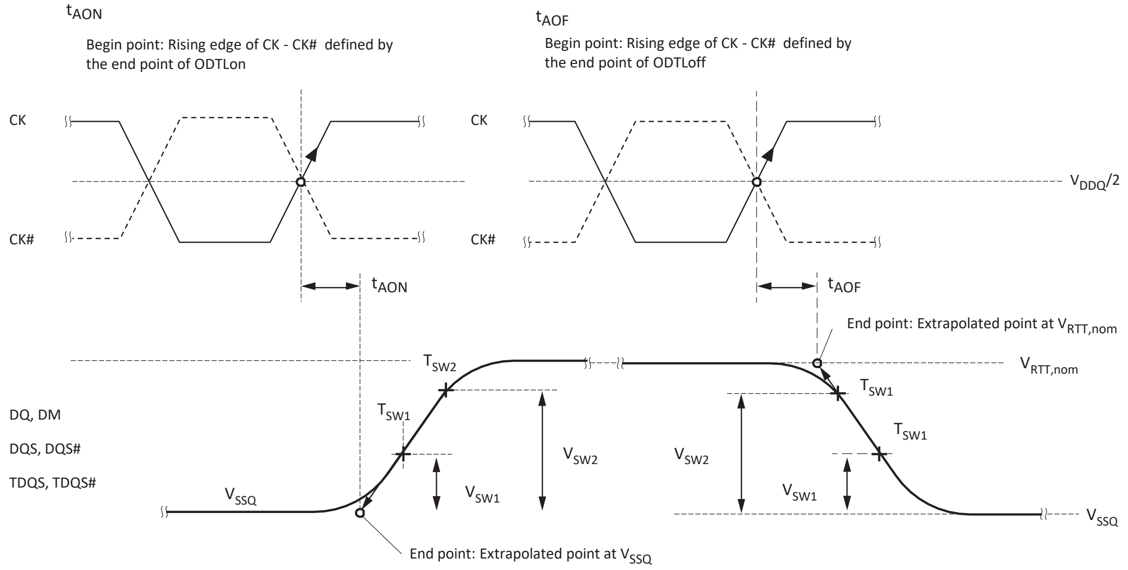


Figure 13 : tAONPD and tAOFPD Definitions

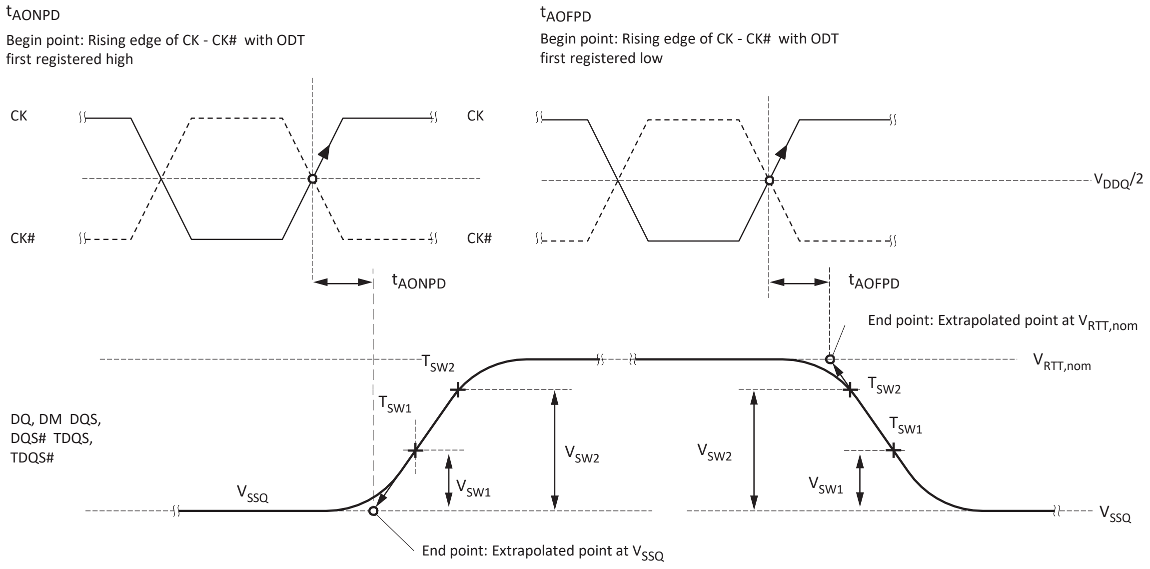
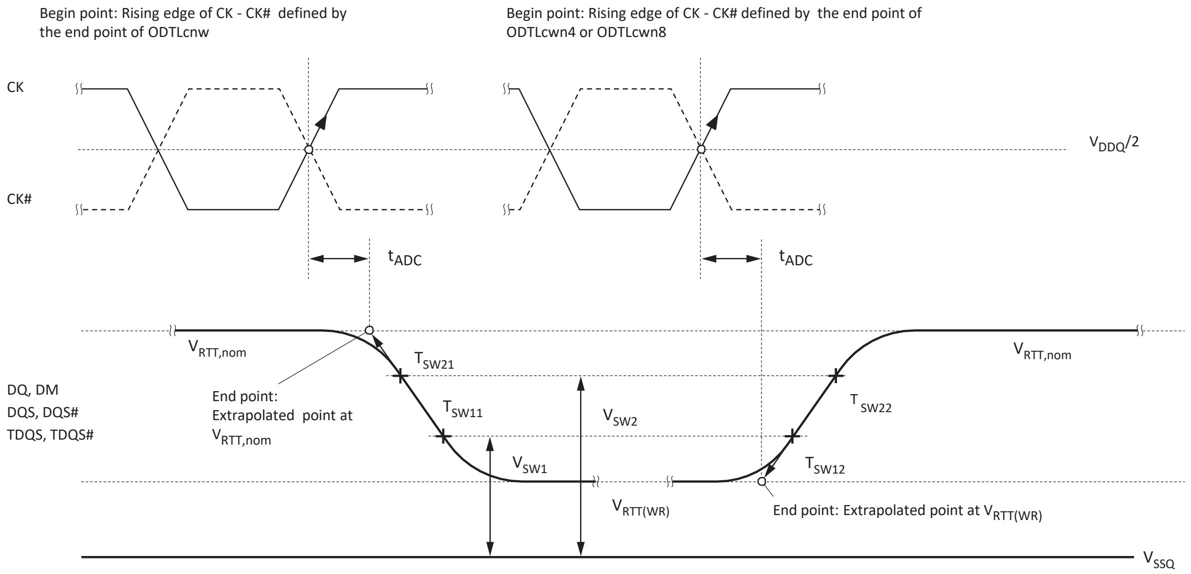


Figure 14 : tADC Definition



Output Driver Impedance

The output driver impedance is selected by MR1[5,1] during initialization. The selected value is able to maintain the tight tolerances specified if proper ZQ calibration is performed. Output specifications refer to the default output driver unless specifically stated otherwise. A functional representation of the output buffer is shown below.

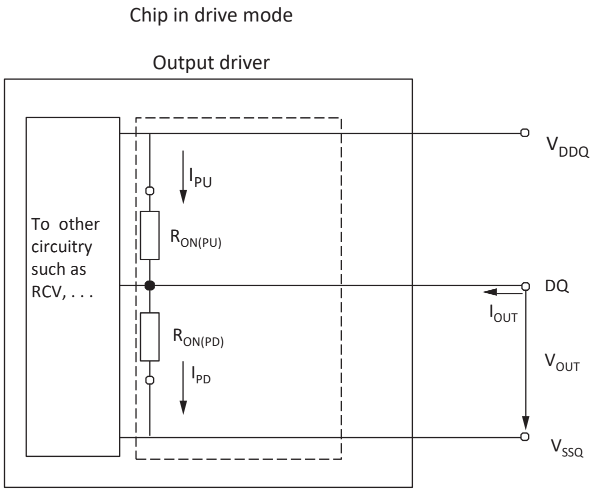
The output driver impedance RON is defined by the value of the external reference resistor RZQ as follows:

- *RON,x* = *RZQ*/*y* (with RZQ = 240Ω±1%; *x=34*Ω or 40Ω with *y* = 7 or 6, respectively)

The individual pull-up and pull-down resistors RON(PU) and RON(PD) are defined as follows:

- *RON(PU)* = (*VDDQ* - *VOUT*)/|*IOUT*|, when RON(PD) is turned off
- *RON(PD)* = (*VOUT*)/|*IOUT*|, when RON(PU) is turned off

Figure 15 : Output Driver



34 Ohm Output Driver Impedance

The 34Ω driver (MR1[5, 1] = 01) is the default driver. Unless otherwise stated, all timings and specifications listed herein apply to the 34Ω driver only. Its impedance RON is defined by the value of the external reference resistor RZQ as follows: RON34 = RZQ/7 (with nominal RZQ = 240Ω ±1%) and is actually 34.3Ω±1%.

Table 31 : 34 Ohm Driver Impedance Characteristics

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Min	Nom	Max	Unit	Notes
0,1	34.3Ω	$R_{ON34(PD)}$	$0.2/V_{DDQ}$	0.6	1.0	1.1	RZQ/7	
			$0.5/V_{DDQ}$	0.9	1.0	1.1	RZQ/7	
			$0.8/V_{DDQ}$	0.9	1.0	1.4	RZQ/7	
		$R_{ON34(PU)}$	$0.2/V_{DDQ}$	0.9	1.0	1.4	RZQ/7	
			$0.5/V_{DDQ}$	0.9	1.0	1.1	RZQ/7	
			$0.8/V_{DDQ}$	0.6	1.0	1.1	RZQ/7	
Pull-up/pull-down mismatch (MM_{PUPD})			$0.5/V_{DDQ}$	–10%	N/A	10	%	2

Notes: 1. Tolerance limits assume RZQ of 240Ω ±1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage: *VDDQ* = *VDD*; *VSSQ* = *VSS*). Refer to 34 Ohm Output Driver Sensitivity if either the temperature or the voltage changes after calibration.

2. Measurement definition for mismatch between pull-up and pull-down (MMPUPD). Measure both RON(PU) and RON(PD) at 0.5 × VDDQ: MMPUPD = × 100 RON(PU) - RON(PD) RON,nom

3. For IT and AT (1Gb only) devices, the minimum values are derated by 6% when the device operates between –40°C and 0°C (TC).

34 Ohm Driver

The 34Ω driver’s current range has been calculated and summarized in Table 33 VDD=1.5V, Table 34 for VDD =1.57V, and Table 35 for VDD=1.42V. The individual pull-up and pull-down resistors RON34(PD) and RON34 (PU)are defined as follows:

- RON34(PD) = (VOUT)/|IOUT|; RON34(PU) is turned off
- RON34(PU) = (VDDQ - VOUT)/|IOUT|; RON34(PD) is turned off

Table 32 : 34 Ohm Driver Pull-Up and Pull-Down Impedance Calculations

R_{ON}				Min	Nom	Max	Unit
RZQ = 240Ω 1%				237.6	240	242.4	Ω
RZQ/7 = (240Ω 1%)/7				33.9	34.3	34.6	Ω
MR1[5,1]	**R_{ON}**	**Resistor**	**V_{OUT}**	**Min**	**Nom**	**Max**	**Unit**
0, 1	34.3Ω	$R_{ON34(PD)}$	0.2 × V_{DDQ}	20.4	34.3	38.1	Ω
			0.5 × V_{DDQ}	30.5	34.3	38.1	Ω
			0.8 × V_{DDQ}	30.5	34.3	48.5	Ω
		$R_{ON34(PU)}$	0.2 × V_{DDQ}	30.5	34.3	48.5	Ω
			0.5 × V_{DDQ}	30.5	34.3	38.1	Ω
			0.8 × V_{DDQ}	20.4	34.3	38.1	Ω

Table 33 : 34 Ohm Driver IOH/IOL Characteristics: VDD = VDDQ = 1.5V

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Max	Nom	Min	Unit
0, 1	34.3Ω	$R_{ON34(PD)}$	I_{OL} @ 0.2 × V_{DDQ}	14.7	8.8	7.9	mA
			I_{OL} @ 0.5 × V_{DDQ}	24.6	21.9	19.7	mA
			I_{OL} @ 0.8 × V_{DDQ}	39.3	35.0	24.8	mA
		$R_{ON34(PU)}$	I_{OH} @ 0.2 × V_{DDQ}	39.3	35.0	24.8	mA
			I_{OH} @ 0.5 × V_{DDQ}	24.6	21.9	19.7	mA
			I_{OH} @ 0.8 × V_{DDQ}	14.7	8.8	7.9	mA

Table 34 : 34 Ohm Driver IOH/IOL Characteristics: VDD = VDDQ = 1.575V

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Max	Nom	Min	Unit
0, 1	34.3Ω	$R_{ON34(PD)}$	I_{OL} @ 0.2 × V_{DDQ}	15.5	9.2	8.3	mA
			I_{OL} @ 0.5 × V_{DDQ}	25.8	23	20.7	mA
			I_{OL} @ 0.8 × V_{DDQ}	41.2	36.8	26	mA
		$R_{ON34(PU)}$	I_{OH} @ 0.2 × V_{DDQ}	41.2	36.8	26	mA
			I_{OH} @ 0.5 × V_{DDQ}	25.8	23	20.7	mA
			I_{OH} @ 0.8 × V_{DDQ}	15.5	9.2	8.3	mA

Table 35: 34 Ohm Driver IOH/IOL Characteristics: VDD = VDDQ = 1.425V

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Max	Nom	Min	Unit
0, 1	34.3Ω	$R_{ON34(PD)}$	I_{OL} @ 0.2 × V_{DDQ}	14.0	8.3	7.5	mA
			I_{OL} @ 0.5 × V_{DDQ}	23.3	20.8	18.7	mA
			I_{OL} @ 0.8 × V_{DDQ}	37.3	33.3	23.5	mA
		$R_{ON34(PU)}$	I_{OH} @ 0.2 × V_{DDQ}	37.3	33.3	23.5	mA
			I_{OH} @ 0.5 × V_{DDQ}	23.3	20.8	18.7	mA
			I_{OH} @ 0.8 × V_{DDQ}	14.0	8.3	7.5	mA

34 Ohm Output Driver Sensitivity

If either the temperature or the voltage changes after ZQ calibration, then the tolerance limits listed in Table 31 can be expected to widen according to Table 36 and Table 37.

Table 36 : 34 Ohm Output Driver Sensitivity Definition

Symbol	Min	Max	Unit
$R_{ON(PD)}$ @ 0.2 × V_{DDQ}	0.6 - $dR_{ON}dTL$ × |ΔT| - $dR_{ON}dVL$ × |ΔV|	1.1 + $dR_{ON}dTL$ × |ΔT| + $dR_{ON}dVL$ × |ΔV|	RZQ/7
$R_{ON(PD)}$ @ 0.5 × V_{DDQ}	0.9 - $dR_{ON}dTM$ × |ΔT| - $dR_{ON}dVM$ × |ΔV|	1.1 + $dR_{ON}dTM$ × |ΔT| + $dR_{ON}dVM$ × |ΔV|	RZQ/7
$R_{ON(PD)}$ @ 0.8 × V_{DDQ}	0.9 - $dR_{ON}dTH$ × |ΔT| - $dR_{ON}dVH$ × |ΔV|	1.4 + $dR_{ON}dTH$ × |ΔT| + $dR_{ON}dVH$ × |ΔV|	RZQ/7
$R_{ON(PU)}$ @ 0.2 × V_{DDQ}	0.9 - $dR_{ON}dTL$ × |ΔT| - $dR_{ON}dVL$ × |ΔV|	1.4 + $dR_{ON}dTL$ × |ΔT| + $dR_{ON}dVL$ × |ΔV|	RZQ/7
$R_{ON(PU)}$ @ 0.5 × V_{DDQ}	0.9 - $dR_{ON}dTM$ × |ΔT| - $dR_{ON}dVM$ × |ΔV|	1.1 + $dR_{ON}dTM$ × |ΔT| + $dR_{ON}dVM$ × |ΔV|	RZQ/7
$R_{ON(PU)}$ @ 0.8 × V_{DDQ}	0.6 - $dR_{ON}dTH$ × |ΔT| - $dR_{ON}dVH$ × |ΔV|	1.1 + $dR_{ON}dTH$ × |ΔT| + $dR_{ON}dVH$ × |ΔV|	RZQ/7

Note : 1. ΔT = *T - T(@CALIBRATION)*, ΔV = *VDDQ - VDDQ(@CALIBRATION)*; and *VDD = VDDQ*.

Table 37 : 34 Ohm Output Driver Voltage and Temperature Sensitivity

Change	Min	Max	Unit
$dR_{ON}dTM$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.13	%/mV
$dR_{ON}dTL$	0	1.5	%/°C
$dR_{ON}dVL$	0	0.13	%/mV
$dR_{ON}dTH$	0	1.5	%/°C
$dR_{ON}dVH$	0	0.13	%/mV

Alternative 40 Ohm Driver

Table 38 : 40 Ohm Driver Impedance Characteristics

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Min	Nom	Max	Unit
0,0	40Ω	$R_{ON40(PD)}$	0.2 × V_{DDQ}	0.6	1.0	1.1	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/6
			0.8 × V_{DDQ}	0.9	1.0	1.4	RZQ/6
		$R_{ON40(PU)}$	0.2 × V_{DDQ}	0.9	1.0	1.4	RZQ/6
			0.5 × V_{DDQ}	0.9	1.0	1.1	RZQ/6
			0.8 × V_{DDQ}	0.6	1.0	1.1	RZQ/6
Pull-up/pull-down mismatch (MM_{PUPD})			0.5 × V_{DDQ}	–10%	N/A	10	%

Notes :
1. Tolerance limits assume RZQ of 240Ω ±1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage (*VDDQ* = *VDD*; *VSSQ* = *VSS*). Refer to 40 Ohm Output Driver Sensitivity if either the temperature or the voltage changes after calibration.
2. Measurement definition for mismatch between pull-up and pull-down (MMPUPD). Measure both RON(PU) and RON (PD) at 0.5 × VDDQ : MMPUPD = (RON(PU) - RON(PD)) / RON,nom × 100
3. For IT and AT (1Gb only) devices, the minimum values are derated by 6% when the device operates between –40°C and 0°C (TC).

40 Ohm Output Driver Sensitivity

If either the temperature or the voltage changes after I/O calibration, then the tolerance limits listed in Table 38 can be expected to widen according to Table 39 and Table 40.

Table 39 : 40 Ohm Output Driver Sensitivity Definition

Symbol	Min	Max	Unit
$R_{ON(PD)}$ @ 0.2 × V_{DDQ}	0.6 - $dR_{ON}dTL$ × |ΔT| - $dR_{ON}dVL$ × |ΔV|	1.1 + $dR_{ON}dTL$ × |ΔT| + $dR_{ON}dVL$ × |ΔV|	RZQ/6
$R_{ON(PD)}$ @ 0.5 × V_{DDQ}	0.9 - $dR_{ON}dTM$ × |ΔT| - $dR_{ON}dVM$ × |ΔV|	1.1 + $dR_{ON}dTM$ × |ΔT| + $dR_{ON}dVM$ × |ΔV|	RZQ/6
$R_{ON(PD)}$ @ 0.8 × V_{DDQ}	0.9 - $dR_{ON}dTH$ × |ΔT| - $dR_{ON}dVH$ × |ΔV|	1.4 + $dR_{ON}dTH$ × |ΔT| + $dR_{ON}dVH$ × |ΔV|	RZQ/6
$R_{ON(PU)}$ @ 0.2 × V_{DDQ}	0.9 - $dR_{ON}dTL$ × |ΔT| - $dR_{ON}dVL$ × |ΔV|	1.4 + $dR_{ON}dTL$ × |ΔT| + $dR_{ON}dVL$ × |ΔV|	RZQ/6
$R_{ON(PU)}$ @ 0.5 × V_{DDQ}	0.9 - $dR_{ON}dTM$ × |ΔT| - $dR_{ON}dVM$ × |ΔV|	1.1 + $dR_{ON}dTM$ × |ΔT| + $dR_{ON}dVM$ × |ΔV|	RZQ/6
$R_{ON(PU)}$ @ 0.8 × V_{DDQ}	0.6 - $dR_{ON}dTH$ × |ΔT| - $dR_{ON}dVH$ × |ΔV|	1.1 + $dR_{ON}dTH$ × |ΔT| + $dR_{ON}dVH$ × |ΔV|	RZQ/6

Note: 1. *ΔT = T - T(@CALIBRATION), ΔV = VDDQ - VDDQ(@CALIBRATION)*; and *VDD = VDDQ*.

Table 40 : 40 Ohm Output Driver Voltage and Temperature Sensitivity

Change	Min	Max	Unit
$dR_{ON}dTM$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	%/mV
$dR_{ON}dTL$	0	1.5	%/°C
$dR_{ON}dVL$	0	0.15	%/mV
$dR_{ON}dTH$	0	1.5	%/°C
$dR_{ON}dVH$	0	0.15	%/mV

Output Characteristics and Operating Conditions

The DRAM uses both single-ended and differential output drivers. The single-ended output driver is summarized below, while the differential output driver is summarized in Table 42.

Table 41 : Single-Ended Output Driver Characteristics

All voltages are referenced to VSS

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output leakage current: DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}; ODT is disabled; ODT is HIGH	I_{OZ}	–5	5	µA	1
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{REF} - 0.1 \times V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.1 \times V_{DDQ}$	SRQ_{se}	2.5	6	V/ns	1, 2, 3, 4
Single-ended DC high-level output voltage	$V_{OH(DC)}$	$0.8 \times V_{DDQ}$		V	1, 2, 5
Single-ended DC mid-point level output voltage	$V_{OM(DC)}$	$0.5 \times V_{DDQ}$		V	1, 2, 5
Single-ended DC low-level output voltage	$V_{OL(DC)}$	$0.2 \times V_{DDQ}$		V	1, 2, 5
Single-ended AC high-level output voltage	$V_{OH(AC)}$	$V_{TT} + 0.1 \times V_{DDQ}$		V	1, 2, 3, 6
Single-ended AC low-level output voltage	$V_{OL(AC)}$	$V_{TT} - 0.1 \times V_{DDQ}$		V	1, 2, 3, 6
Delta R_{ON} between pull-up and pull-down for DQ/DQS	MM_{PUPD}	–10	10	%	1, 7
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				3

Notes :
1. RZQ of 240Ω ±1% with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (*VDDQ=VDD*; *VSSQ=VSS*).
2. *VTT* = *VDDQ*/2.
3. See Figure 18 for the test load configuration.
4. The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching in the opposite direction. For all other DQ signal switching combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.
5. See Table 31 for IV curve linearity. Do not use AC test load.
6. See Table 43 for output slew rate.
7. See Table 31 for additional information.
8. See Figure 16 for an example of a single-ended output signal.

Table 42: Differential Output Driver Characteristics

All voltages are referenced to VSS

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output leakage current: DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}; ODT is disabled; ODT is HIGH	I_{OZ}	–5	5	µA	1
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)} = –0.2 × V_{DDQ}$ and $V_{OH,diff(AC)} = +0.2 × V_{DDQ}$	SRQ_{diff}	5	12	V/ns	1
Output differential cross-point voltage	$V_{OX(AC)}$	V_{REF} - 150	V_{REF} + 150	mV	1, 2, 3
Differential high-level output voltage	$V_{OH,diff(AC)}$	+0.2 × V_{DDQ}		V	1, 4
Differential low-level output voltage	$V_{OL,diff(AC)}$	–0.2 × V_{DDQ}		V	1, 4
Delta R_{ON} between pull-up and pull-down for DQ/DQS	MM_{PUPD}	–10	10	%	1, 5
Test load for AC timing and output slew rates	Output to V_{TT} (V_{DDQ}/2) via 25Ω resistor				3

Notes :
1. RZQ of 240Ω ±1% with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (*VDDQ* = *VDD*; *VSSQ* = *VSS*).
2. *VREF* = *VDDQ*/2; slew rate @ 5 V/ns, interpolate for faster slew rate.
3. See Figure 18 for the test load configuration.
4. See Table 44 for the output slew rate.
5. See Table 31 for additional information.
6. See Figure 17 for an example of a differential output signal.

Figure 16 : DQ Output Signal

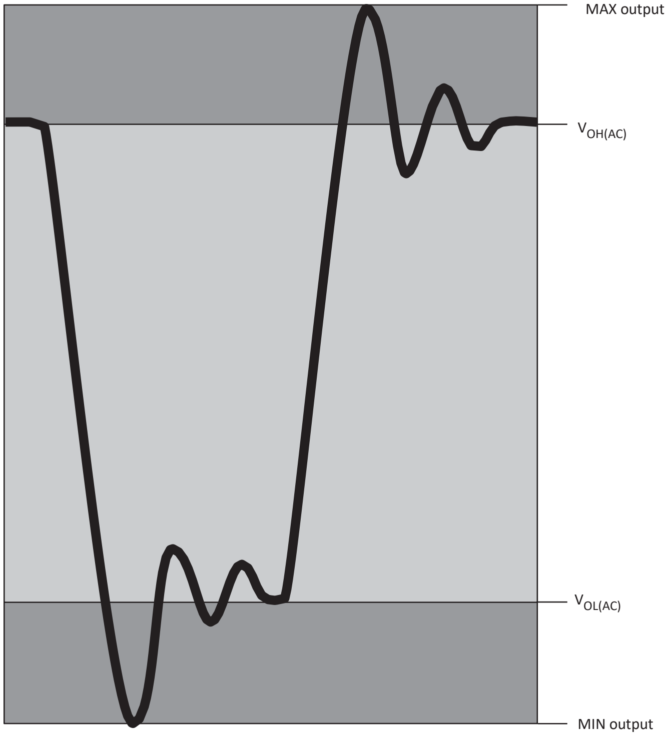
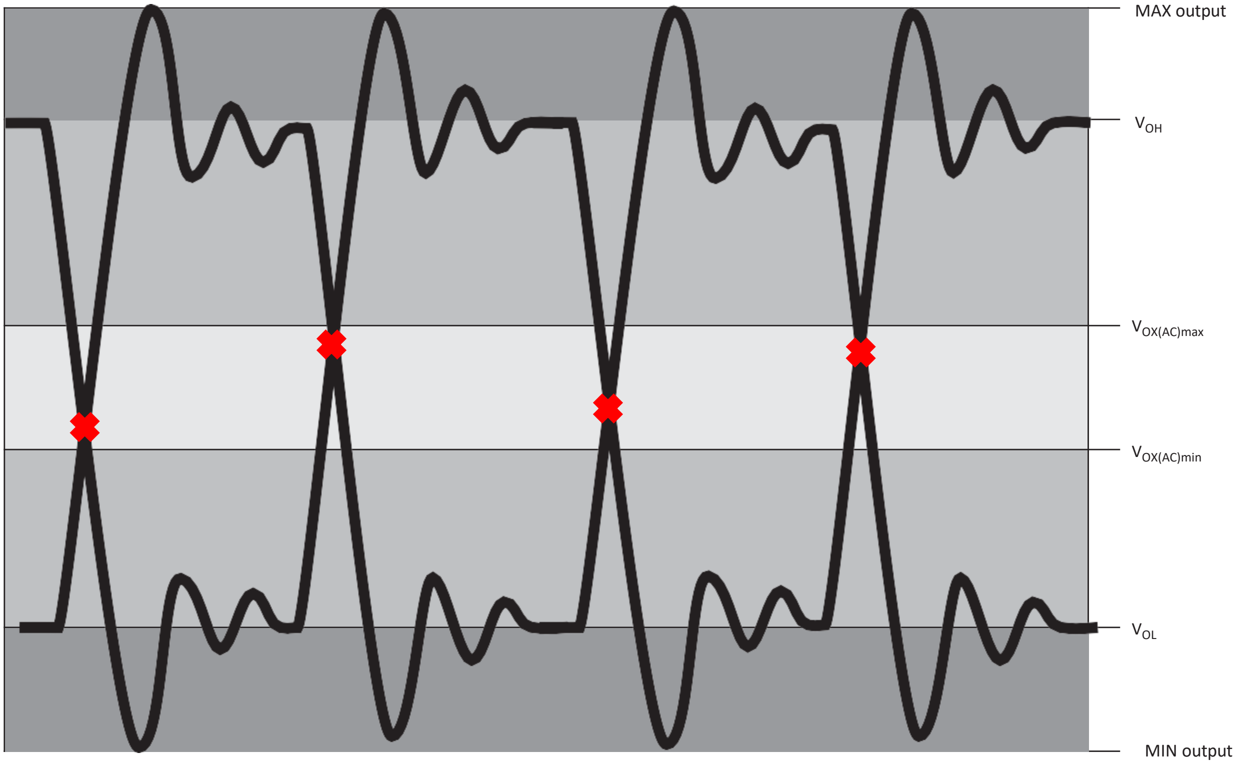


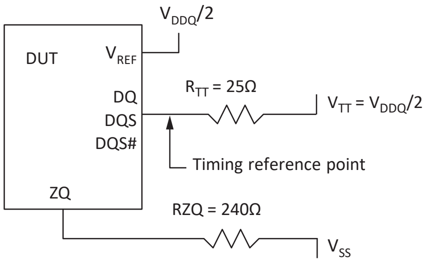
Figure 17 : Differential Output Signal



Reference Output Load

Figure 18 represents the effective reference load of 25Ω used in defining the relevant device AC timing parameters (except ODT reference timing) as well as the output slew rate measurements. It is not intended to be a precise representation of a particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment.

Figure 18 : Reference Output Load for AC Timing and Output Slew Rate



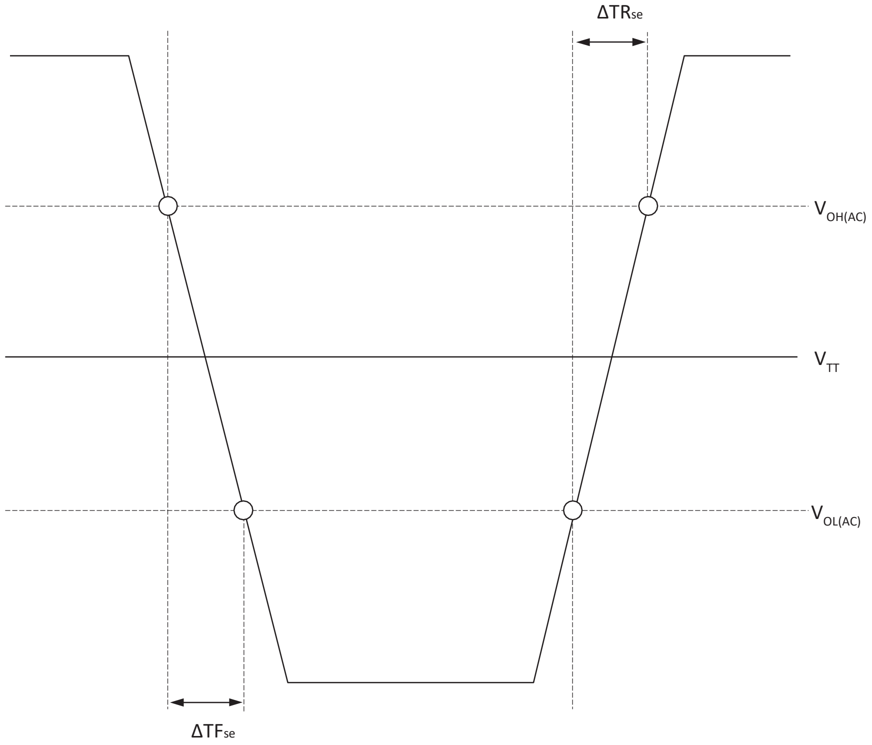
Slew Rate Definitions for Single-Ended Output Signals

The single-ended output driver is summarized in Table 41. With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single-ended signals.

Table 43 : Single-Ended Output Slew Rate Definition

Single-Ended Output Slew Rates (Linear Signals)		Measured		Calculation
Output	Edge	From	To	
DQ	Rising	$V_{OL(AC)}$	$V_{OH(AC)}$	$\frac{V_{OH(AC)} - V_{OL(AC)}}{\Delta TR_{se}}$
	Falling	$V_{OH(AC)}$	$V_{OL(AC)}$	$\frac{V_{OH(AC)} - V_{OL(AC)}}{\Delta TF_{se}}$

Figure 19 : Nominal Slew Rate Definition for Single-Ended Output Signals



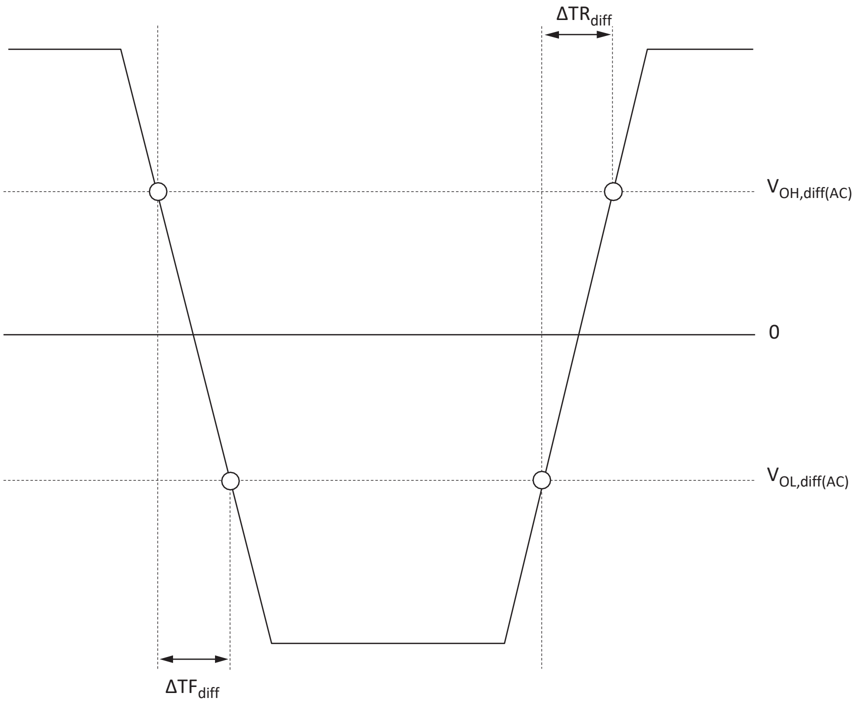
Slew Rate Definitions for Differential Output Signals

The differential output driver is summarized in Table 42. With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for differential signals.

Table 44 : Single-Ended Output Slew Rate Definition

Differential Output Slew Rates (Linear Signals)		Measured		Calculation
Output	Edge	From	To	
DQS, DQS#	Rising	$V_{OL,diff(AC)}$	$V_{OH,diff(AC)}$	$\frac{V_{OH,diff(AC)} - V_{OL,diff(AC)}}{\Delta TR_{diff}}$
	Falling	$V_{OH,diff(AC)}$	$V_{OL,diff(AC)}$	$\frac{V_{OH,diff(AC)} - V_{OL,diff(AC)}}{\Delta TF_{diff}}$

Figure 20 : Nominal Differential Output Slew Rate Definition for DQS, DQS#



Speed Bin Tables

Table 45 : DDR3-1066 Speed Bins

DDR3-1066 Speed Bin			-5F		-5G		Unit	Notes
CL-^{t}RCD-^{t}RP			7-7-7		8-8-8			
Parameter		Symbol	Min	Max	Min	Max		
Internal READ command to first data		^{t}AA	13.125	–	15	–	ns	
ACTIVATE to internal READ or WRITE delay time		^{t}RCD	13.125	–	15	–	ns	
PRECHARGE command period		^{t}RP	13.125	–	15	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		^{t}RC	50.625	–	52.5	–	ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	37.5	9 x ^{t}REFI	37.5	9 x ^{t}REFI	ns	1
CL = 5	CWL = 5	^{t}CK (AVG)	3.0	3.3	3.0	3.3	ns	2
	CWL = 6	^{t}CK (AVG)	Reserved		Reserved		ns	3
CL = 6	CWL = 5	^{t}CK (AVG)	2.5	3.3	2.5	3.3	ns	2
	CWL = 6	^{t}CK (AVG)	Reserved		Reserved		ns	3
CL = 7	CWL = 5	^{t}CK (AVG)	Reserved		Reserved		ns	3
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	Reserved		ns	2,3
CL = 8	CWL = 5	^{t}CK (AVG)	Reserved		Reserved		ns	3
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	1.875	<2.5	ns	2
Supported CL settings			5, 6, 7, 8		5, 6, 8		CK	
Supported CWL settings			5, 6		5, 6		CK	

Notes : 1. ^{t}REFI depends on T_{OPER}.

2. The CL and CWL settings result in ^{t}CK requirements. When making a selection ^{t}CK, both CL and CWL requirement settings need to be fulfilled.

3. Reserved settings are not allowed.

Table 46 : DDR3-1333 Speed Bins

DDR3-1333 Speed Bin			-6H[1]		-6J[2]		Unit	Notes
CL-^{t}RCD-^{t}RP			9-9-9		10-10-10			
Parameter		Symbol	Min	Max	Min	Max		
Internal READ command to first data		^{t}AA	13.5	–	15	–	ns	
ACTIVATE to internal READ or WRITE delay time		^{t}RCD	13.5	–	15	–	ns	
PRECHARGE command period		^{t}RP	13.5	–	15	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		^{t}RC	49.5	–	51	–	ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	36	9 x ^{t}REFI	36	9 x ^{t}REFI	ns	3
CL = 5	CWL = 5	^{t}CK (AVG)	3.0	3.3	3.0	3.3	ns	4
	CWL = 6, 7	^{t}CK (AVG)	Reserved		Reserved		ns	5
CL = 6	CWL = 5	^{t}CK (AVG)	2.5	3.3	2.5	3.3	ns	4
	CWL = 6	^{t}CK (AVG)	Reserved		Reserved		ns	5
	CWL = 7	^{t}CK (AVG)	Reserved		Reserved		ns	5
CL = 7	CWL = 5	^{t}CK (AVG)	Reserved		Reserved		ns	5
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	Reserved		ns	4,5
	CWL = 7	^{t}CK (AVG)	Reserved		Reserved		ns	5
CL = 8	CWL = 5	^{t}CK (AVG)	Reserved		Reserved		ns	5
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	1.875	<2.5	ns	4
	CWL = 7	^{t}CK (AVG)	Reserved		Reserved		ns	5
CL = 9	CWL = 5, 6	^{t}CK (AVG)	Reserved		Reserved		ns	5
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	Reserved		ns	4,5
CL = 10	CWL = 5, 6	^{t}CK (AVG)	Reserved		Reserved		ns	5
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	1.5	<1.875	ns	4
Supported CL settings			5, 6, 7, 8, 9, 10		5, 6, 8, 10		CK	
Supported CWL settings			5, 6, 7		5, 6, 7		CK	

Notes :
1. The -6H speed grade is backward compatible with 1066, CL = 7 (-5F).
2. The -6J speed grade is backward compatible with 1066, CL = 8 (-5G).
3. ^{t}REFI depends on T_{OPER}.
4. The CL and CWL settings result in ^{t}CK requirements. When making a selection of ^{t}CK, both CL and CWL requirement settings need to be fulfilled.
5. Reserved settings are not allowed

Table 47 : DDR3-1600 Speed Bins

DDR3-1600 Speed Bin			-8K[1]		Unit	Notes
CL-^{t}RCD-^{t}RP			11-11-11			
Parameter		Symbol	Min	Max		
Internal READ command to first data		^{t}AA	13.75	–	ns	
ACTIVATE to internal READ or WRITE delay time		^{t}RCD	13.75	–	ns	
PRECHARGE command period		^{t}RP	13.75	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		^{t}RC	48.75	–	ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	35	9 x ^{t}REFI	ns	2
CL = 5	CWL = 5	^{t}CK (AVG)	3.0	3.3	ns	3
	CWL = 6, 7, 8	^{t}CK (AVG)	Reserved		ns	4
CL = 6	CWL = 5	^{t}CK (AVG)	2.5	3.3	ns	3
	CWL = 6	^{t}CK (AVG)	Reserved		ns	4
	CWL = 7, 8	^{t}CK (AVG)	Reserved		ns	4
CL = 7	CWL = 5	^{t}CK (AVG)	Reserved		ns	4
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	ns	3
	CWL = 7	^{t}CK (AVG)	Reserved		ns	4
	CWL = 8	^{t}CK (AVG)	Reserved		ns	4
CL = 8	CWL = 5	^{t}CK (AVG)	Reserved		ns	4
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	ns	3
	CWL = 7	^{t}CK (AVG)	Reserved		ns	4
	CWL = 8	^{t}CK (AVG)	Reserved		ns	4
CL = 9	CWL = 5, 6	^{t}CK (AVG)	Reserved		ns	4
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	ns	3
	CWL = 8	^{t}CK (AVG)	Reserved		ns	4
CL = 10	CWL = 5, 6	^{t}CK (AVG)	Reserved		ns	4
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	ns	3
	CWL = 8	^{t}CK (AVG)	Reserved		ns	4
CL = 11	CWL = 5, 6, 7	^{t}CK (AVG)	Reserved		ns	4
	CWL = 8	^{t}CK (AVG)	1.25	<1.5	ns	3
Supported CL settings			5, 6, 7, 8, 9, 10, 11		CK	
Supported CWL settings			5, 6, 7, 8		CK	

Notes : 1. The -8K speed grade is backward compatible with 1333, CL = 9 (-6H) and 1066, CL = 7 (-6J).

2. . ^{t}REFI depends on T_{OPER}.

3. The CL and CWL settings result in ^{t}CK requirements. When making a selection of ^{t}CK , both CL and CWL requirement settings need to be fulfilled.

4. Reserved settings are not allowed.

Table 48 : DDR3-1866 Speed Bins

DDR3-1866 Speed Bin			-9M[1]		Unit	Notes
CL-^{t}RCD-^{t}RP			13-13-13			
Parameter		Symbol	Min	Max		
Internal READ command to first data		^{t}AA	13.91	20		
ACTIVATE to internal READ or WRITE delay time		^{t}RCD	13.91	–	ns	
PRECHARGE command period		^{t}RP	13.91	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		^{t}RC	47.91	–	ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	34	9 x ^{t}REFI	ns	2
CL = 5	CWL = 5	^{t}CK (AVG)	3.0	3.3	ns	3
	CWL = 6, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	4
CL = 6	CWL = 5	^{t}CK (AVG)	2.5	3.3	ns	3
	CWL = 6, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	4
CL = 7	CWL = 5, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	4
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	ns	3
CL = 8	CWL = 5, 8, 9	^{t}CK (AVG)	Reserved		ns	4
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	ns	3
	CWL = 7	^{t}CK (AVG)	Reserved		ns	4
CL = 9	CWL = 5, 6, 8, 9	^{t}CK (AVG)	Reserved		ns	4
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	ns	3
CL = 10	CWL = 5, 6, 9	^{t}CK (AVG)	Reserved		ns	4
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	ns	3
	CWL = 8	^{t}CK (AVG)	Reserved		ns	4
CL = 11	CWL = 5, 6, 7	^{t}CK (AVG)	Reserved		ns	4
	CWL = 8	^{t}CK (AVG)	1.25	<1.5	ns	3
	CWL = 9	^{t}CK (AVG)	Reserved		ns	4
CL = 12	CWL = 5, 6, 7, 8	^{t}CK (AVG)	Reserved		ns	4
	CWL = 9	^{t}CK (AVG)	Reserved		ns	4
CL = 13	CWL = 5, 6, 7, 8	^{t}CK (AVG)	Reserved		ns	4
	CWL = 9	^{t}CK (AVG)	1.07	<1.25	ns	3
Supported CL settings			5, 6, 7, 8, 9, 10, 11, 13		CK	
Supported CWL settings			5, 6, 7, 8, 9		CK	

Notes :

1. The -9M speed grade is backward compatible with 1600, CL = 11 (-8K); 1333, CL = 9 (-6H); and 1066, CL = 7 (-5F).
2. ^{t}REFI depends on T_{OPER}.
3. The CL and CWL settings result in ^{t}CK requirements. When making a selection of ^{t}CK, both CL and CWL requirement settings need to be fulfilled.
4. Reserved settings are not allowed.

Table 49 : DDR3-2133 Speed Bins

DDR3-2133 Speed Bin			-AN[1]		Unit	Notes
CL-^{t}RCD-^{t}RP			14-14-14			
Parameter		Symbol	Min	Max		
Internal READ command to first data		^{t}AA	13.09	20		
ACTIVATE to internal READ or WRITE delay time		^{t}RCD	13.09	–	ns	
PRECHARGE command period		^{t}RP	13.09	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		^{t}RC	46.09	–	ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	33	9 x ^{t}REFI	ns	2
CL = 5	CWL = 5	^{t}CK (AVG)	3.0	3.3	ns	3
	CWL = 6, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	4
CL = 6	CWL = 5	^{t}CK (AVG)	2.5	3.3	ns	3
	CWL = 6, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	4
CL = 7	CWL = 5, 7, 8, 9	^{t}CK (AVG)	Reserved		ns	4
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	ns	3
CL = 8	CWL = 5, 8, 9	^{t}CK (AVG)	Reserved		ns	4
	CWL = 6	^{t}CK (AVG)	1.875	<2.5	ns	3
	CWL = 7	^{t}CK (AVG)	Reserved		ns	4
CL = 9	CWL = 5, 6, 8, 9	^{t}CK (AVG)	Reserved		ns	4
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	ns	3
CL = 10	CWL = 5, 6, 9	^{t}CK (AVG)	Reserved		ns	4
	CWL = 7	^{t}CK (AVG)	1.5	<1.875	ns	3
	CWL = 8	^{t}CK (AVG)	Reserved		ns	4
CL = 11	CWL = 5, 6, 7	^{t}CK (AVG)	Reserved		ns	4
	CWL = 8	^{t}CK (AVG)	1.25	<1.5	ns	3
	CWL = 9	^{t}CK (AVG)	Reserved		ns	4
CL = 12	CWL = 5, 6, 7, 8	^{t}CK (AVG)	Reserved		ns	4
	CWL = 9	^{t}CK (AVG)	Reserved		ns	4
CL = 13	CWL = 5, 6, 7, 8	^{t}CK (AVG)	Reserved		ns	4
	CWL = 9	^{t}CK (AVG)	1.07	<1.25	ns	3
CL = 14	CWL = 5, 6, 7, 8, 9	^{t}CK (AVG)	Reserved	Reserved	ns	4
	CWL = 10	^{t}CK (AVG)	0.938	<1.07	ns	3
Supported CL settings			5, 6, 7, 8, 9, 10, 11, 13, 14		CK	
Supported CWL settings			5, 6, 7, 8, 9		CK	

Notes :
1. The -AN speed grade is backward compatible with 1866, CL = 13 (-9M); 1600, CL = 11 (-8K); 1333, CL = 9 (-6H); and 1066, CL = 7 (-5F).
2. ^{t}REFI depends on T_{OPER}.
3. The CL and CWL settings result in ^{t}CK requirements. When making a selection of tCK, both CL and CWL requirement settings need to be fulfilled.
4. Reserved settings are not allowed.

Electrical Characteristics and AC Operating Conditions

Table 50: Electrical Characteristics and AC Operating Conditions

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing												
Clock period average: DLL disable mode	$T_C \leq 85°C$	^{t}CK	8	7800	8	7800	8	7800	8	7800	ns	9, 42
	T_C = >85°C to 95°C	(DLL_DIS)	8	3900	8	3900	8	3900	8	3900	ns	42
Clock period average: DLL enable mode		^{t}CK (AVG)	See Speed Bin Tables for ^{t}CK range allowed								ns	10, 11
High pulse width average		^{t}CH (AVG)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	CK	12
Low pulse width average		^{t}CL (AVG)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	CK	12
Clock period jitter	DLL locked	^{t}JITper	–100	100	–90	90	–80	80	–70	70	ps	13
	DLL locking	^{t}JITper,lck	–90	90	–80	80	–70	70	–60	60	ps	13
Clock absolute period		^{t}CK (ABS)	MIN = ^{t}CK (AVG) MIN + ^{t}JITper MIN; MAX = ^{t}CK (AVG) MAX + ^{t}JITper MAX								ps	
Clock absolute high pulse width		^{t}CH (ABS)	0.43	–	0.43	–	0.43	–	0.43	–	^{t}CK (AVG)	14
Clock absolute low pulse width		^{t}CL (ABS)	0.43	–	0.43	–	0.43	–	0.43	–	^{t}CK (AVG)	15
Cycle-to-cycle jitter	DLL locked	^{t}JITcc	200		180		160		140		ps	16
	DLL locking	^{t}JITcc,lck	180		160		140		120		ps	16
Cumulative error across	2 cycles	^{t}ERR2per	–147	147	–132	132	–118	118	–103	103	ps	17
	3 cycles	^{t}ERR3per	–175	175	–157	157	–140	140	–122	122	ps	17
	4 cycles	^{t}ERR4per	–194	194	–175	175	–155	155	–136	136	ps	17
	5 cycles	^{t}ERR5per	–209	209	–188	188	–168	168	–147	147	ps	17
	6 cycles	^{t}ERR6per	–222	222	–200	200	–177	177	–155	155	ps	17
	7 cycles	^{t}ERR7per	–232	232	–209	209	–186	186	–163	163	ps	17
	8 cycles	^{t}ERR8per	–241	241	–217	217	–193	193	–169	169	ps	17
	9 cycles	^{t}ERR9per	–249	249	–224	224	–200	200	–175	175	ps	17
	10 cycles	^{t}ERR10per	–257	257	–231	231	–205	205	–180	180	ps	17
	11 cycles	^{t}ERR11per	–263	263	–237	237	–210	210	–184	184	ps	17
	12 cycles	^{t}ERR12per	–269	269	–242	242	–215	215	–188	188	ps	17
	n = 13, 14 . . . 49, 50 cycles	^{t}ERR$n$per	^{t}ERR$n$per MIN = (1 + 0.68ln[n]) × ^{t}JITper MIN tERRnper MAX = (1 + 0.68ln[n]) × tJITper MAX								ps	17

Table 50 : Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
DQ Input Timing												
Data setup time to DQS, DQS#	Base (specification)	^{t}DS (AC175)	75	–	25	–	–	–	–	–	ps	18, 19, 44
	V_{REF} @ 1 V/ns		250	–	200	–	–	–	–	–	ps	19, 20
Data setup time to DQS, DQS#	Base (specification)	^{t}DS (AC150)	125	–	75	–	30	–	10	–	ps	18, 19, 44
	V_{REF} @ 1 V/ns		275	–	250	–	180	–	160	–	ps	19, 20
Data setup time to DQS, DQS#	Base (specification)	^{t}DS (AC135)	–	–	–	–	–	–	–	–	ps	18, 19
	V_{REF} @ 1 V/ns		–	–	–	–	–	–	–	–	ps	19, 20
Data hold time from DQS, DQS#	Base (specification)	^{t}DH (DC100)	150	–	100	–	65	–	45	–	ps	18, 19
	V_{REF} @ 1 V/ns		250	–	200	–	165	–	145	–	ps	19, 20
Minimum data pulse width		^{t}DIPW	600	–	490	–	400	–	360	–	ps	41
DQ Output Timing												
DQS, DQS# to DQ skew, per access		^{t}DQSQ	–	200	–	150	–	125	–	100	ps	
DQ output hold time from DQS, DQS#		^{t}QH	0.38	–	0.38	–	0.38	–	0.38	–	^{t}CK (AVG)	21
DQ Low-Z time from CK, CK#		^{t}LZDQ	–800	400	–600	300	–500	250	–450	225	ps	22, 23
DQ High-Z time from CK, CK#		^{t}HZDQ	–	400	–	300	–	250	–	225	ps	22, 23
DQ Strobe Input Timing												
DQS, DQS# rising to CK, CK# rising		^{t}DQSS	–0.25	0.25	–0.25	0.25	–0.25	0.25	–0.27	0.27	CK	25
DQS, DQS# differential input low pulse width		^{t}DQSL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	CK	
DQS, DQS# differential input high pulse width		^{t}DQSH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	CK	
DQS, DQS# falling setup to CK, CK# rising		^{t}DSS	0.2	–	0.2	–	0.2	–	0.2	–	CK	25
DQS, DQS# falling hold from CK, CK# rising		^{t}DSH	0.2	–	0.2	–	0.2	–	0.2	–	CK	25
DQS, DQS# differential WRITE preamble		^{t}WPRE	0.9	–	0.9	–	0.9	–	0.9	–	CK	
DQS, DQS# differential WRITE postamble		^{t}WPST	0.3	–	0.3	–	0.3	–	0.3	–	CK	
DQ Strobe Output Timing												
DQS, DQS# rising to/from rising CK, CK#		^{t}DQSCK	–400	400	–300	300	–255	255	–225	225	ps	23
DQS, DQS# rising to/from rising CK, CK# when DLL is disabled		^{t}DQSCK (DLL_DIS)	1	10	1	10	1	10	1	10	ns	26

Table 50 : Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
DQS, DQS# differential output high time		^{t}QSH	0.38	–	0.38	–	0.40	–	0.40	–	CK	21
DQS, DQS# differential output low time		^{t}QSL	0.38	–	0.38	–	0.40	–	0.40	–	CK	21
DQS, DQS# Low-Z time (RL - 1)		^{t}LZDQS	–800	400	–600	300	–500	250	–450	225	ps	22, 23
DQS, DQS# High-Z time (RL + BL/2)		^{t}HZDQS	–	400	–	300	–	250	–	225	ps	22, 23
DQS, DQS# differential READ preamble		^{t}RPRE	0.9	Note 24	0.9	Note 24	0.9	Note 24	0.9	Note 24	CK	23, 24
DQS, DQS# differential READ postamble		^{t}RPST	0.3	Note 27	0.3	Note 27	0.3	Note 27	0.3	Note 27	CK	23, 27
Command and Address Timing												
DLL locking time		^{t}DLLK	512	–	512	–	512	–	512	–	CK	28
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	^{t}IS (AC175)	200	–	125	–	65	–	45	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		375	–	300	–	240	–	220	–	ps	20, 30
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	^{t}IS (AC150)	350	–	275	–	190	–	170	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		500	–	425	–	340	–	320	–	ps	20, 30
CTRL, CMD, ADDR hold from CK,CK#	Base (specification)	^{t}IH (DC100)	275	–	200	–	140	–	120	–	ps	29, 30
	V_{REF} @ 1 V/ns		375	–	300	–	240	–	220	–	ps	20, 30
Minimum CTRL, CMD, ADDR pulse width		^{t}IPW	900	–	780	–	620	–	560	–	ps	41
ACTIVATE to internal READ or WRITE delay		^{t}RCD	See Speed Bin Tables for ^{t}RCD								ns	31
PRECHARGE command period		^{t}RP	See Speed Bin for ^{t}RP								ns	31
ACTIVATE-to-PRECHARGE command period		^{t}RAS	See Speed Bin Tables for ^{t}RAS								ns	31, 32
ACTIVATE-to-ACTIVATE command period		^{t}RC	See Speed Bin Tables for ^{t}RC								ns	31, 43
ACTIVATE-to-ACTIVATE minimum command period	x4/x8 (1KB page size)	^{t}RRD	MIN = greater of 4CK or 10ns		MIN = greater of 4CK or 7.5ns		MIN = greater of 4CK or 6ns		MIN = greater of 4CK or 6ns		CK	31
	x16 (2KB page size)		MIN = greater of 4CK or 10ns				MIN = greater of 4CK or 7.5ns				CK	31
Four ACTIVATE windows	x4/x8 (1KB page size)	^{t}FAW	40	–	37.5	–	30	–	30	–	ns	31
	x16 (2KB page size)		50	–	50	–	45	–	40	–	ns	31
Write recovery time		^{t}WR	MIN = 15ns; MAX = N/A								ns	31, 32, 33, 34
Delay from start of internal WRITE transaction to internal READ command		^{t}WTR	MIN = greater of 4CK or 7.5ns; MAX = N/A								CK	31, 34

Table 50 : Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
READ-to-PRECHARGE time		^{t}RTP	MIN = greater of 4CK or 7.5ns; MAX = N/A								CK	31, 32
CAS#-to-CAS# command delay		^{t}CCD	MIN = 4CK; MAX = N/A								CK	
Auto precharge write recovery + precharge time		^{t}DAL	MIN = WR + ^{t}RP/^{t}CK (AVG); MAX = N/A								CK	
MODE REGISTER SET command cycle time		^{t}MRD	MIN = 4CK; MAX = N/A								CK	
MODE REGISTER SET command update delay		^{t}MOD	MIN = greater of 12CK or 15ns; MAX = N/A								CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		^{t}MPRR	MIN = 1CK; MAX = N/A								CK	
Calibration Timing												
ZQCL command: Long calibration time	POWER-UP and RESET operation	^{t}ZQinit	512	–	512	–	512	–	512	–	CK	
	Normal operation	^{t}ZQoper	256	–	256	–	256	–	256	–	CK	
ZQCS command: Short calibration time		^{t}ZQCS	64	–	64	–	64	–	64	–	CK	
Initialization and Reset Timing												
Exit reset from CKE HIGH to a valid command		^{t}XPR	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = N/A								CK	
Begin power supply ramp to power supplies stable		^{t}VDDPR	MIN = N/A; MAX = 200								ms	
RESET# LOW to power supplies stable		^{t}RPS	MIN = 0; MAX = 200								ms	
RESET# LOW to I/O and R_{TT} High-Z		^{t}IOZ	MIN = N/A; MAX = 20								ns	35
Refresh Timing												
REFRESH-to-ACTIVATE or REFRESH command period		^{t}RFC – 1Gb	MIN = 110; MAX = 70,200								ns	
		^{t}RFC – 2Gb	MIN = 160; MAX = 70,200								ns	
		^{t}RFC – 4Gb	MIN = 260; MAX = 70,200								ns	
		^{t}RFC – 8Gb	MIN = 350; MAX = 70,200								ns	
Maximum refresh period	$T_C \le 85°C$	–	64 (1X)								ms	36
	$T_C > 85°C$		32 (2X)								ms	36
Maximum average periodic refresh	$T_C \le 85°C$	^{t}REFI	7.8 (64ms/8192)								µs	36
	$T_C > 85°C$		3.9 (32ms/8192)								µs	36
Self Refresh Timing												

Table 50 : Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Exit self refresh to commands not requiring a locked DLL		^{t}XS	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = N/A								CK	
Exit self refresh to commands requiring a locked DLL		^{t}XSDLL	MIN = ^{t}DLLK (MIN); MAX = N/A								CK	28
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		^{t}CKESR	MIN = ^{t}CKE (MIN) + CK; MAX = N/A								CK	
Valid clocks after self refresh entry or power-down entry		^{t}CKSRE	MIN = greater of 5CK or 10ns; MAX = N/A								CK	
Valid clocks before self refresh exit, power-down exit, or reset exit		^{t}CKSRX	MIN = greater of 5CK or 10ns; MAX = N/A								CK	
Power-Down Timing												
CKE MIN pulse width		^{t}CKE (MIN)	Greater of 3CK or 7.5ns		Greater of 3CK or 5.625ns		Greater of 3CK or 5.625ns		Greater of 3CK or 5ns		CK	
Command pass disable delay		^{t}CPDED	MIN = 1; MAX = N/A								CK	
Power-down entry to power-down exit timing		^{t}PD	MIN = ^{t}CKE (MIN); MAX = 9 * tREFI								CK	
Begin power-down period prior to CKE registered HIGH		^{t}ANPD	WL - 1CK								CK	
Power-down entry period: ODT either synchronous or asynchronous		PDE	Greater of ^{t}ANPD or ^{t}RFC - REFRESH command to CKE LOW time								CK	
Power-down exit period: ODT either synchronous or asynchronous		PDX	^{t}ANPD + ^{t}XPDLL								CK	
Power-Down Entry Minimum Timing												
ACTIVATE command to power-down entry		^{t}ACTPDEN	MIN = 1								CK	
PRECHARGE/PRECHARGE ALL command to power-down entry		^{t}PRPDEN	MIN = 1								CK	
REFRESH command to power-down entry		^{t}REFPDEN	MIN = 1								CK	37
MRS command to power-down entry		^{t}MRSPDEN	MIN = ^{t}MOD (MIN)								CK	
READ/READ with auto precharge command to power-down entry		^{t}RDPDEN	MIN = RL + 4 + 1								CK	
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRPDEN	MIN = WL + 4 + ^{t}WR/^{t}CK (AVG)								CK	
	BC4MRS	^{t}WRPDEN	MIN = WL + 2 + tWR/tCK (AVG)								CK	

Table 50 : Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRAP-DEN	MIN = WL + 4 + WR + 1								CK	
	BC4MRS	^{t}WRAP-DEN	MIN = WL + 2 + WR + 1								CK	
Power-Down Exit Timing												
DLL on, any valid command, or DLL off to commands not requiring locked DLL		^{t}XP	MIN = greater of 3CK or 7.5ns; MAX = N/A				MIN = greater of 3CK or 6ns; MAX = N/A				CK	
Precharge power-down with DLL off to commands requiring a locked DLL		^{t}XPDLL	MIN = greater of 10CK or 24ns; MAX = N/A								CK	28
ODT Timing												
R_{TT} synchronous turn-on delay		ODTLon	CWL + AL - 2CK								CK	38
R_{TT} synchronous turn-off delay		ODTLoff	CWL + AL - 2CK								CK	40
R_{TT} turn-on from ODTL on reference		^{t}AON	–400	400	–300	300	–250	250	–225	225	ps	23, 38
R_{TT} turn-off from ODTL off reference		^{t}AOF	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	CK	39, 40
Asynchronous R_{TT} turn-on delay (power-down with DLL off)		^{t}AONPD	MIN = 2; MAX = 8.5								ns	38
Asynchronous R_{TT} turn-off delay (power-down with DLL off)		^{t}AOFPD	`MIN = 2; MAX = 8.5								ns	40
ODT HIGH time with WRITE command and BL8		ODTH8	MIN = 6; MAX = N/A								CK	
ODT HIGH time without WRITE command or with WRITE command and BC4		ODTH4	MIN = 4; MAX = N/A								CK	
Dynamic ODT Timing												
$R_{TT,nom}$-to-$R_{TT(WR)}$ change skew		ODTLcnw	WL - 2CK								CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BC4		ODTLcwn4	4CK + ODTLoff								CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BL8		ODTLcwn8	6CK + ODTLoff								CK	
R_{TT} dynamic change skew		^{t}ADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	CK	39
Write Leveling Timing												
First DQS, DQS# rising edge		^{t}WLMRD	40	–	40	–	40	–	40	–	CK	
DQS, DQS# delay		^{t}WLDQSEN	25	–	25	–	25	–	25	–	CK	
Write leveling setup from rising CK, CK# crossing to rising DQS, DQS# crossing		^{t}WLS	325	–	245	–	195	–	165	–	ps	

Table 50 : Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write leveling hold from rising DQS, DQS# crossing to rising CK, CK# crossing	^{t}WLH	325	–	245	–	195	–	165	–	ps	
Write leveling output delay	^{t}WLO	0	9	0	9	0	9	0	8	ns	
Write leveling output error	^{t}WLOE	0	2	0	2	0	2	0	2	ns	

Notes :

1. AC timing parameters are valid from specified T_C MIN to T_C MAX values.
2. All voltages are referenced to VSS.
3. Output timings are only valid for R_{ON34} output buffer selection.
4. The unit tCK (AVG) represents the actual tCK (AVG) of the input clock under operation. The unit CK represents one clock cycle of the input clock, counting the actual clock edges.
5. AC timing and I_{DD} tests may use a V_{IL} -to- V_{IH} swing of up to 900mV in the test environment, but input timing is still referenced to V_{REF} (except tIS, tIH, tDS, and tDH use the AC/DC trip points and CK, CK# and DQS, DQS# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs and 2 V/ns for differential inputs in the range between $V_{IL(AC)}$ and $V_{IHAC)}$.
6. All timings that use time-based values (ns, µs, ms) should use tCK (AVG) to determine the correct number of clocks (Table51 uses CK or tCK [AVG] interchangeably). In the case of noninteger results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.
7. Strobe or DQS_{diff} refers to the DQS and DQS# differential crossing point when DQS is the rising edge. Clock or CK refers to the CK and CK# differential crossing point when CK is the rising edge.
8. This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. he output signal voltage reference point is VDDQ/2 for single-ended signals and the crossing point for differential signals (see Figure 18).
9. When operating in DLL disable mode, Dosilicon does not warrant compliance with normal mode timings or functionality.
10. The clock's tCK (AVG) is the average clock over any 200 consecutive clocks and tCK (AVG) MIN is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
11. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spreadspectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of tCK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below tCK (AVG) MIN.
12. The clock's tCH (AVG) and tCL (AVG) are the average half clock period over any 200 consecutive clocks and is the smallest clock half period allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
13. The period jitter (tJITper) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.
14. tCH (ABS) is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.
15. tCL (ABS) is the absolute instantaneous clock low pulse width as measured from one falling edge to the following rising edge.
16. The cycle-to-cycle jitter tJITcc is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.
17. The cumulative jitter error tERRnper, where *n* is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over *n* number of clock cycles.
18. tDS (base) and tDH (base) values are for a single-ended 1 V/ns slew rate DQs and 2 V/ns slew rate differential DQS, DQS#.
19. These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transition edge to its respective data strobe signal (DQS, DQS#) crossing.
20. The setup and hold times are listed converting the base specification values (to which derating tables apply) to VREF when the slew rate is 1 V/ns. These values, with a slew rate of 1 V/ns, are for reference only.
21. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJITper (larger of tJITper (MIN) or tJITper (MAX) of the input clock (output deratings are relative to the SDRAM input clock).
22. Single-ended signal parameter.
23. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The following parameters are required to be derated by subtracting tERR10per (MAX): tDQSCK (MIN), tLZDQS (MIN), tLZDQ (MIN), and tAON (MIN). The following parameters are required to be derated by subtracting tERR10per (MIN) : tDQSCK (MAX), tHZ (MAX), tLZDQS (MAX), tLZDQ MAX, and tAON (MAX). The parameter tRPRE(MIN) is derated by subtracting tJITper (MAX), while tRPRE (MAX) is derated by subtracting tJITper (MIN).
24. The maximum preamble is bound by tLZDQS (MAX).

25. These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its respective clock signal (CK, CK#) crossing. The specification values are not affected by the amount of clock jitter applied, as these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present.
26. The tDQSCK (DLL_DIS) parameter begins CL + AL - 1 cycles after the READ command.
27. The maximum postamble is bound by tHZDQS (MAX).
28. Commands requiring a locked DLL are: READ (and RDAP) and synchronous ODT commands. In addition, after any change of latency tXPDLL, timing must be met.
29. tIS (base) and tIH (base) values are for a single-ended 1 V/ns control/command/address slew rate and 2 V/ns CK, CK# differential slew rate.
30. These parameters are measured from a command/address signal transition edge to its respective clock (CK, CK#) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present.
31. For these parameters, the DDR3 SDRAM device supports t*n*PARAM (*n*CK) = RU(tPARAM [ns]/tCK[AVG] [ns]), assuming all input clock jitter specifications are satisfied. For example, the device will support t*n*RP (*n*CK)=RU(tRP/tCK [AVG]) if all input clock jitter specifications are met. This means that for DDR3-800 6-6-6, of which tRP = 5ns, the device will support t*n*RP = RU(tRP/tCK[AVG]) = 6 as long as the input clock jitter specifications are met. That is, the PRECHARGE command at T0 and the ACTIVATE command at T0 + 6 are valid even if six clocks are less than 15ns due to input clock jitter.
32. During READs and WRITEs with auto precharge, the DDR3 SDRAM will hold off the internal PRECHARGE command until tRAS (MIN) has been satisfied.
33. When operating in DLL disable mode, the greater of 4CK or 15ns is satisfied for tWR.
34. The start of the write recovery time is defined as follows:
    - For BL8 (fixed by MRS or OTF): Rising clock edge four clock cycles after WL
    - For BC4 (OTF): Rising clock edge four clock cycles after WL
    - For BC4 (fixed by MRS): Rising clock edge two clock cycles after WL
35. RESET# should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until RESET# is LOW, the outputs are at risk of driving and could result in excessive current, depending on bus activity.
36. The refresh period is 64ms when TC is less than or equal to 85°C. This equates to an average refresh rate of 7.8125µs. However, nine REFRESH commands should be asserted at least once every 70.3µs. When TC is greater than 85°C, the refresh period is 32ms.
37. Although CKE is allowed to be registered LOW after a REFRESH command when tREFPDEN (MIN) is satisfied, there are cases where additional time such as tXPDLL (MIN) is required.
38. ODT turn-on time MIN is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on. The ODT reference load is shown in Figure 10. Designs that were created prior to JEDEC tightening the maximum limit from 9ns to 8.5ns will be allowed to have a 9ns maximum.
39. Half-clock output parameters must be derated by the actual tERR10per and tJITdty when input clock jitter is present. This results in each parameter becoming larger. The parameters tADC (MIN) and tAOF (MIN) are each required to be derated by subtracting both tERR10per (MAX) and tJITdty (MAX). The parameters tADC (MAX) and tAOF (MAX) are required to be derated by subtracting both tERR10per (MAX) and tJITdty (MAX).
40. ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn-off time maximum is when the DRAM buffer is in High-Z. The ODT reference load is shown in Figure 11. This output load is used for ODT timings (see Figure 18).
41. Pulse width of a input signal is defined as the width between the first crossing of $V_{REF(DC)}$ and the consecutive crossing of $V_{REF(DC)}$.
42. Should the clock rate be larger than tRFC (MIN), an AUTO REFRESH command should have at least one NOP command between it and another AUTO REFRESH command. Additionally, if the clock rate is slower than 40ns(25 MHz), all REFRESH commands should be followed by a PRECHARGE ALL command.
43. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in a reduction of REFRESH characteristics or product lifetime.
44. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs. For example, for DDR3-800, two input AC levels are defined : $V_{IH(AC175),min}$ and $V_{IH(AC150),min}$ (corresponding $V_{IL(AC175),min}$ and $V_{IL(AC150),min}$. For DDR3-800, the address/ command inputs must use either $V_{IH(AC175),min}$ with tIS(AC175) of 200ps or $V_{IH(150),min}$ with tIS(AC150) of 350ps; independently, the data inputs must use either $V_{IH(AC175),min}$ with tDS(AC175) of 75ps or $V_{IH(AC150),min}$ with tDS(AC150) of 125ps.

Electrical Characteristics and AC Operating Conditions

Table 51 : Electrical Characteristics and AC Operating Conditions for Speed Extensions

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3-1866		DDR3-2133		Unit	Notes
			Min	Max	Min	Max		
Clock Timing								
Clock period average: DLL disable mode	T_C = 0°C to 85°C	^tCK	8	7800	8	7800	ns	9, 42
	T_C = >85°C to 95°C	(DLL_DIS)	8	3900	8	3900	ns	42
Clock period average: DLL enable mode		^tCK (AVG)	See Speed Bin Tables for tCK range allowed				ns	10, 11
High pulse width average		^tCH (AVG)	0.47	0.53	0.47	0.53	CK	12
Low pulse width average		^tCL (AVG)	0.47	0.53	0.47	0.53	CK	12
Clock period jitter	DLL locked	^tJITper	–60	60	–50	50	ps	13
	DLL locking	$^tJITper,lck$	–50	50	–40	40	ps	13
Clock absolute period		^tCK (ABS)	MIN = ^tCK (AVG) MIN + tJITper MIN; MAX = tCK (AVG) MAX + tJITper MAX				ps	
Clock absolute high pulse width		^tCH (ABS)	0.43	–	0.43	–	^tCK (AVG)	14
Clock absolute low pulse width		^tCL (ABS)	0.43	–	0.43	–	^tCK (AVG)	15
Cycle-to-cycle jitter	DLL locked	^tJITcc	120		120		ps	16
	DLL locking	$^tJITcc,lck$	100		100		ps	16

Table 51 : Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3-1866		DDR3-2133		Unit	Notes
			Min	Max	Min	Max		
Cumulative error across	2 cycles	^{t}ERR2per	–88	88	-74	74	ps	17
	3 cycles	^{t}ERR3per	–105	105	-87	87	ps	17
	4 cycles	^{t}ERR4per	–117	117	-97	97	ps	17
	5 cycles	^{t}ERR5per	–126	126	-105	105	ps	17
	6 cycles	^{t}ERR6per	–133	133	-111	111	ps	17
	7 cycles	^{t}ERR7per	–139	139	-116	116	ps	17
	8 cycles	^{t}ERR8per	–145	145	-121	121	ps	17
	9 cycles	^{t}ERR9per	–150	150	-125	125	ps	17
	10 cycles	^{t}ERR10per	–154	154	-128	128	ps	17
	11 cycles	^{t}ERR11per	–158	158	-132	132	ps	17
	12 cycles	^{t}ERR12per	–161	161	-134	134	ps	17
	n = 13, 14 . . . 49, 50 cycles	^{t}ERR*n*per	^{t}ERR*n*per MIN = (1 + 0.68ln[*n*]) × ^{t}JITper MIN tERRnper MAX = (1 + 0.68ln[n]) × tJITper MAX				ps	17
DQ Input Timing								
Data setup time to DQS, DQS#	Base (specification) @ 2 V/ns	^{t}DS (AC135)	68	–	53	–	ps	18, 19
	V_{REF} @ 2 V/ns		135	–	121	–	ps	19, 20
Data hold time from DQS, DQS#	Base (specification) @ 2 V/ns	^{t}DH (DC100)	70	–	55	–	ps	18, 19
	V_{REF} @ 2 V/ns		120	–	105	–	ps	19, 20
Minimum data pulse width		^{t}DIPW	320	–	280	–	ps	41
DQ Output Timing								
DQS, DQS# to DQ skew, per access		^{t}DQSQ	–	85	–	75	ps	
DQ output hold time from DQS, DQS#		^{t}QH	0.38	–	0.38	–	^{t}CK (AVG)	21
DQ Low-Z time from CK, CK#		^{t}LZDQ	–390	195	–360	180	ps	22, 23
DQ High-Z time from CK, CK#		^{t}HZDQ	–	195	–	180	ps	22, 23
DQ Strobe Input Timing								
DQS, DQS# rising to CK, CK# rising		^{t}DQSS	–0.27	0.27	–0.27	0.27	CK	25

Table 51 : Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3-1866		DDR3-2133		Unit	Notes
			Min	Max	Min	Max		
DQS, DQS# differential input low pulse width		^{t}DQSL	0.45	0.55	0.45	0.55	CK	
DQS, DQS# differential input high pulse width		^{t}DQSH	0.45	0.55	0.45	0.55	CK	
DQS, DQS# falling setup to CK, CK# rising		^{t}DSS	0.2	–	0.2	–	CK	25
DQS, DQS# falling hold from CK, CK# rising		^{t}DSH	0.2	–	0.2	–	CK	25
DQS, DQS# differential WRITE preamble		^{t}WPRE	0.9	–	0.9	–	CK	
DQS, DQS# differential WRITE postamble		^{t}WPST	0.3	–	0.3	–	CK	
DQ Strobe Output Timing								
DQS, DQS# rising to/from rising CK, CK#		^{t}DQSCK	–195	195	–180	180	ps	23
DQS, DQS# rising to/from rising CK, CK# when DLL is disabled		^{t}DQSCK (DLL_DIS)	1	10	1	10	ns	26
DQS, DQS# differential output high time		^{t}QSH	0.40	–	0.40	–	CK	21
DQS, DQS# differential output low time		^{t}QSL	0.40	–	0.40	–	CK	21
DQS, DQS# Low-Z time (RL - 1)		^{t}LZDQS	–390	195	–360	180	ps	22, 23
DQS, DQS# High-Z time (RL + BL/2)		^{t}HZDQS	–	195	–	180	ps	22, 23
DQS, DQS# differential READ preamble		^{t}RPRE	0.9	Note 24	0.9	Note 24	CK	23, 24
DQS, DQS# differential READ postamble		^{t}RPST	0.3	Note 27	0.3	Note 27	CK	23, 27
Command and Address Timing								
DLL locking time		^{t}DLLK	512	–	512	–	CK	28
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	^{t}IS (AC135)	65	–	60	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		200	–	195	–	ps	20, 30
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	^{t}IS (AC125)	150	–	135	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		275	–	260	–	ps	20, 30
CTRL, CMD, ADDR hold from CK,CK#	Base (specification)	^{t}IH (DC100)	100	–	95	–	ps	29, 30
	V_{REF} @ 1 V/ns		200	–	195	–	ps	20, 30
Minimum CTRL, CMD, ADDR pulse width		^{t}IPW	535	–	470	–	ps	41
ACTIVATE to internal READ or WRITE delay		^{t}RCD	See Speed Bin Tables for tRCD				ns	31
PRECHARGE command period		^{t}RP	See Speed Bin Tables for tRP				ns	31
ACTIVATE-to-PRECHARGE command period		^{t}RAS	See Speed Bin Tables for tRAS				ns	31, 32

Table 51 : Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3-1866		DDR3-2133		Unit	Notes
			Min	Max	Min	Max		
ACTIVATE-to-ACTIVATE command period		^{t}RC	See Speed Bin Tables for ^{t}RC				ns	31, 43
ACTIVATE-to-ACTIVATE minimum command period	1KB page size	^{t}RRD	MIN = greater of 4CK or 5ns				CK	31
	2KB page size		MIN = greater of 4CK or 6ns				CK	31
Four ACTIVATE windows	1KB page size	^{t}FAW	27	–	25	–	ns	31
	2KB page size		35	–	35	–	ns	31
Write recovery time		^{t}WR	MIN = 15ns; MAX = N/A				ns	31, 32, 33
Delay from start of internal WRITE transaction to internal READ command		^{t}WTR	MIN = greater of 4CK or 7.5ns; MAX = N/A				CK	31, 34
READ-to-PRECHARGE time		^{t}RTP	MIN = greater of 4CK or 7.5ns; MAX = N/A				CK	31, 32
CAS#-to-CAS# command delay		^{t}CCD	MIN = 4CK; MAX = N/A				CK	
Auto precharge write recovery + precharge time		^{t}DAL	MIN = WR + ^{t}RP/^{t}CK (AVG); MAX = N/A				CK	
MODE REGISTER SET command cycle time		^{t}MRD	MIN = 4CK; MAX = N/A				CK	
MODE REGISTER SET command update delay		^{t}MOD	MIN = greater of 12CK or 15ns; MAX = N/A				CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		^{t}MPRR	MIN = 1CK; MAX = N/A				CK	
Calibration Timing								
ZQCL command: Long calibration time	POWER-UP and RESET operation	^{t}ZQinit	MIN = N/A MAX = max(512nCK, 640ns)				CK	
	Normal operation	^{t}ZQoper	MIN = N/A MAX = max(256nCK, 320ns)				CK	
ZQCS command: Short calibration time		^{t}ZQCS	MIN = N/A MAX = max(64nCK, 80ns)				CK	
Initialization and Reset Timing								
Exit reset from CKE HIGH to a valid command		^{t}XPR	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = N/A				CK	
Begin power supply ramp to power supplies stable		^{t}VDDPR	MIN = N/A; MAX = 200				ms	
RESET# LOW to power supplies stable		^{t}RPS	MIN = 0; MAX = 200				ms	
RESET# LOW to I/O and R_{TT} High-Z		^{t}IOZ	MIN = N/A; MAX = 20				ns	35

Table 51 : Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3-1866		DDR3-2133		Unit	Notes
			Min	Max	Min	Max		
Refresh Timing								
REFRESH-to-ACTIVATE or REFRESH command period		^{t}RFC – 1Gb	MIN = 110; MAX = 70,200				ns	
		^{t}RFC – 2Gb	MIN = 160; MAX = 70,200				ns	
		^{t}RFC – 4Gb	MIN = 260; MAX = 70,200				ns	
		^{t}RFC – 8Gb	MIN = 350; MAX = 70,200				ns	
Maximum refresh period	$T_C \leq 85°C$	–	64 (1X)				ms	36
	$T_C > 85°C$		32 (2X)				ms	36
Maximum average periodic refresh	$T_C \leq 85°C$	^{t}REFI	7.8 (64ms/8192)				µs	36
	$T_C > 85°C$		3.9 (32ms/8192)				µs	36
Self Refresh Timing								
Exit self refresh to commands not requiring a locked DLL		^{t}XS	MIN = greater of 5CK or ^{t}RFC + 10ns; MAX = N/A				CK	
Exit self refresh to commands requiring a locked DLL		^{t}XSDLL	MIN = ^{t}DLLK (MIN); MAX = N/A				CK	28
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		^{t}CKESR	MIN = ^{t}CKE (MIN) + CK; MAX = N/A				CK	
Valid clocks after self refresh entry or power-down entry		^{t}CKSRE	MIN = greater of 5CK or 10ns; MAX = N/A				CK	
Valid clocks before self refresh exit, power-down exit, or reset exit		^{t}CKSRX	MIN = greater of 5CK or 10ns; MAX = N/A				CK	
Power-Down Timing								
CKE MIN pulse width		^{t}CKE (MIN)	Greater of 3CK or 5ns				CK	
Command pass disable delay		^{t}CPDED	MIN = 2; MAX = N/A				CK	
Power-down entry to power-down exit timing		^{t}PD	MIN = ^{t}CKE (MIN); MAX = 9 * tREFI				CK	
Begin power-down period prior to CKE registered HIGH		^{t}ANPD	WL - 1CK				CK	
Power-down entry period: ODT either synchronous or asynchronous		PDE	Greater of ^{t}ANPD or ^{t}RFC - REFRESH command to CKE LOW time				CK	
Power-down exit period: ODT either synchronous or asynchronous		PDX	^{t}ANPD + ^{t}XPDLL				CK	

Table 51 : Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3-1866		DDR3-2133		Unit	Notes
			Min	Max	Min	Max		
Power-Down Entry Minimum Timing								
ACTIVATE command to power-down entry		^{t}ACTPDEN	MIN = 2				CK	
PRECHARGE/PRECHARGE ALL command to power-down entry		^{t}PRPDEN	MIN = 2				CK	
REFRESH command to power-down entry		^{t}REFPDEN	MIN = 2				CK	37
MRS command to power-down entry		^{t}MRSPDEN	MIN = ^{t}MOD (MIN)				CK	
READ/READ with auto precharge command to power-down entry		^{t}RDPDEN	MIN = RL + 4 + 1				CK	
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRPDEN	MIN = WL + 4 + tWR/tCK (AVG)				CK	
	BC4MRS	^{t}WRPDEN	MIN = WL + 2 + tWR/tCK (AVG)				CK	
WRITE with auto pre-charge command to power-down entry	BL8 (OTF, MRS) BC4OTF	^{t}WRAP-DEN	MIN = WL + 4 + WR + 1				CK	
	BC4MRS	^{t}WRAP-DEN	MIN = WL + 2 + WR + 1				CK	
Power-Down Exit Timing								
DLL on, any valid command, or DLL off to commands not requiring locked DLL		^{t}XP	MIN = greater of 3CK or 6ns; MAX = N/A				CK	
Precharge power-down with DLL off to commands requiring a locked DLL		^{t}XPDLL	MIN = greater of 10CK or 24ns; MAX = N/A				CK	28
ODT Timing								
R_{TT} synchronous turn-on delay		ODTL on	CWL + AL - 2CK				CK	38
R_{TT} synchronous turn-off delay		ODTL off	CWL + AL - 2CK				CK	40
R_{TT} turn-on from ODTL on reference		^{t}AON	–195	195	–180	180	ps	23, 38
R_{TT} turn-off from ODTL off reference		^{t}AOF	0	0.7	0	0.7	CK	39, 40
Asynchronous R_{TT} turn-on delay (power-down with DLL off)		^{t}AONPD	MIN = 2; MAX = 8.5				ns	38
Asynchronous R_{TT} turn-off delay (power-down with DLL off)		^{t}AOFPD	MIN = 2; MAX = 8.5				ns	40
ODT HIGH time with WRITE command and BL8		ODTH8	MIN = 6; MAX = N/A				CK	

Table 51 : Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter	Symbol	DDR3-1866		DDR3-2133		Unit	Notes
		Min	Max	Min	Max		
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4	MIN = 4; MAX = N/A				CK	
Dynamic ODT Timing							
$R_{TT,nom}$-to-$R_{TT(WR)}$ change skew	ODTLcnw	WL - 2CK				CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BC4	ODTLcwn4	4CK + ODTLoff				CK	
$R_{TT(WR)}$-to-$R_{TT,nom}$ change skew - BL8	ODTLcwn8	6CK + ODTLoff				CK	
R_{TT} dynamic change skew	^{t}ADC	0.3	1	0.3	1	CK	39
Write Leveling Timing							
First DQS, DQS# rising edge	^{t}WLMRD	40	–	40	–	CK	
DQS, DQS# delay	^{t}WLDQSEN	25	–	25	–	CK	
Write leveling setup from rising CK, CK# crossing to rising DQS, DQS# crossing	^{t}WLS	140	–	125	–	ps	
Write leveling hold from rising DQS, DQS# crossing to rising CK, CK# crossing	^{t}WLH	140	–	125	–	ps	
Write leveling output delay	^{t}WLO	0	7.5	0	7	ns	
Write leveling output error	^{t}WLOE	0	2	0	2	ns	

Notes :

1. AC timing parameters are valid from specified T_C MIN to T_C MAX values.
2. All voltages are referenced to VSS.
3. Output timings are only valid for R_{ON34} output buffer selection.
4. The unit tCK (AVG) represents the actual tCK (AVG) of the input clock under operation. The unit CK represents one clock cycle of the input clock, counting the actual clock edges.
5. AC timing and I_{DD} tests may use a V_{IL} -to- V_{IH} swing of up to 900mV in the test environment, but input timing is still referenced to V_{REF} (except tIS, tIH, tDS, and tDH use the AC/DC trip points and CK, CK# and DQS, DQS# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs and 2 V/ns for differential inputs in the range between $V_{IL(AC)}$ and $V_{IHAC)}$.
6. All timings that use time-based values (ns, µs, ms) should use tCK (AVG) to determine the correct number of clocks (Table51 uses CK or tCK [AVG] interchangeably). In the case of noninteger results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.
7. Strobe or DQS_{diff} refers to the DQS and DQS# differential crossing point when DQS is the rising edge. Clock or CK refers to the CK and CK# differential crossing point when CK is the rising edge.
8. This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. he output signal voltage reference point is VDDQ/2 for single-ended signals and the crossing point for differential signals (see Figure 18).
9. When operating in DLL disable mode, Dosilicon does not warrant compliance with normal mode timings or functionality.
10. The clock’s tCK (AVG) is the average clock over any 200 consecutive clocks and tCK (AVG) MIN is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
11. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spreadspectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of tCK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below tCK (AVG) MIN.
12. The clock’s tCH (AVG) and tCL (AVG) are the average half clock period over any 200 consecutive clocks and is the smallest clock half period allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
13. The period jitter (tJITper) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.
14. tCH (ABS) is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.
15. tCL (ABS) is the absolute instantaneous clock low pulse width as measured from one falling edge to the following rising edge.
16. The cycle-to-cycle jitter tJITcc is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.
17. The cumulative jitter error tERRnper, where *n* is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over *n* number of clock cycles.
18. tDS (base) and tDH (base) values are for a single-ended 1 V/ns slew rate DQs and 2 V/ns slew rate differential DQS, DQS#.
19. These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transition edge to its respective data strobe signal (DQS, DQS#) crossing.
20. The setup and hold times are listed converting the base specification values (to which derating tables apply) to VREF when the slew rate is 1 V/ns. These values, with a slew rate of 1 V/ns, are for reference only.
21. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJITper (larger of tJITper (MIN) or tJITper (MAX) of the input clock (output deratings are relative to the SDRAM input clock).
22. Single-ended signal parameter.
23. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The following parameters are required to be derated by subtracting tERR10per (MAX): tDQSCK (MIN), tLZDQS (MIN), tLZDQ (MIN), and tAON (MIN). The following parameters are required to be derated by subtracting tERR10per (MIN) : tDQSCK (MAX), tHZ (MAX), tLZDQS (MAX), tLZDQ MAX, and tAON (MAX). The parameter tRPRE(MIN) is derated by subtracting tJITper (MAX), while tRPRE (MAX) is derated by subtracting tJITper (MIN).
24. The maximum preamble is bound by tLZDQS (MAX).

25. These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its respective clock signal (CK, CK#) crossing. The specification values are not affected by the amount of clock jitter applied, as these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present.
26. The tDQSCK (DLL_DIS) parameter begins CL + AL - 1 cycles after the READ command.
27. The maximum postamble is bound by tHZDQS (MAX).
28. Commands requiring a locked DLL are: READ (and RDAP) and synchronous ODT commands. In addition, after any change of latency tXPDLL, timing must be met.
29. tIS (base) and tIH (base) values are for a single-ended 1 V/ns control/command/address slew rate and 2 V/ns CK, CK# differential slew rate.
30. These parameters are measured from a command/address signal transition edge to its respective clock (CK, CK#) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present.
31. For these parameters, the DDR3 SDRAM device supports t*n*PARAM (*n*CK) = RU(tPARAM [ns]/tCK[AVG] [ns]), assuming all input clock jitter specifications are satisfied. For example, the device will support t*n*RP (*n*CK)=RU(tRP/tCK [AVG]) if all input clock jitter specifications are met. This means that for DDR3-800 6-6-6, of which tRP = 5ns, the device will support t*n*RP = RU(tRP/tCK[AVG]) = 6 as long as the input clock jitter specifications are met. That is, the PRECHARGE command at T0 and the ACTIVATE command at T0 + 6 are valid even if six clocks are less than 15ns due to input clock jitter.
32. During READs and WRITEs with auto precharge, the DDR3 SDRAM will hold off the internal PRECHARGE command until tRAS (MIN) has been satisfied.
33. When operating in DLL disable mode, the greater of 4CK or 15ns is satisfied for tWR.
34. The start of the write recovery time is defined as follows:
    - For BL8 (fixed by MRS or OTF): Rising clock edge four clock cycles after WL
    - For BC4 (OTF): Rising clock edge four clock cycles after WL
    - For BC4 (fixed by MRS): Rising clock edge two clock cycles after WL
35. RESET# should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until RESET# is LOW, the outputs are at risk of driving and could result in excessive current, depending on bus activity.
36. The refresh period is 64ms when TC is less than or equal to 85°C. This equates to an average refresh rate of 7.8125µs. However, nine REFRESH commands should be asserted at least once every 70.3µs. When TC is greater than 85°C, the refresh period is 32ms.
37. Although CKE is allowed to be registered LOW after a REFRESH command when tREFPDEN (MIN) is satisfied, there are cases where additional time such as tXPDLL (MIN) is required.
38. ODT turn-on time MIN is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on. The ODT reference load is shown in Figure 10. Designs that were created prior to JEDEC tightening the maximum limit from 9ns to 8.5ns will be allowed to have a 9ns maximum.
39. Half-clock output parameters must be derated by the actual tERR10per and tJITdty when input clock jitter is present. This results in each parameter becoming larger. The parameters tADC (MIN) and tAOF (MIN) are each required to be derated by subtracting both tERR10per (MAX) and tJITdty (MAX). The parameters tADC (MAX) and tAOF (MAX) are required to be derated by subtracting both tERR10per (MAX) and tJITdty (MAX).
40. ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn-off time maximum is when the DRAM buffer is in High-Z. The ODT reference load is shown in Figure 11. This output load is used for ODT timings (see Figure 18).
41. Pulse width of a input signal is defined as the width between the first crossing of $V_{REF(DC)}$ and the consecutive crossing of $V_{REF(DC)}$.
42. Should the clock rate be larger than tRFC (MIN), an AUTO REFRESH command should have at least one NOP command between it and another AUTO REFRESH command. Additionally, if the clock rate is slower than 40ns(25 MHz), all REFRESH commands should be followed by a PRECHARGE ALL command.
43. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in a reduction of REFRESH characteristics or product lifetime.
44. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs. For example, for DDR3-800, two input AC levels are defined : $V_{IH(AC175),min}$ and $V_{IH(AC150),min}$ (corresponding $V_{IL(AC175),min}$ and $V_{IL(AC150),min}$. For DDR3-800, the address/ command inputs must use either $V_{IH(AC175),min}$ with tIS(AC175) of 200ps or $V_{IH(150),min}$ with tIS(AC150) of 350ps; independently, the data inputs must use either $V_{IH(AC175),min}$ with tDS(AC175) of 75ps or $V_{IH(AC150),min}$ with tDS(AC150) of 125ps.

Command and Address Setup, Hold, and Derating

The total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS (base) and tIH (base) values (see Table 53; values come from Table 51 to the ΔtIS and ΔtIH derating values (see Table 54 and Table 55), respectively.
Example: tIS (total setup time) = tIS (base) + ΔtIS. For a valid transition, the input signal has to remain above/below VIH(AC)/VIL(AC) for some time tVAC (see Table 55).

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached VIH(AC)/VIL(AC) at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach VIH(AC)/VIL(AC) (see Figure 2) for input signal requirements). For slew rates that fall between the values listed in Table 55 and Table 58 , the derating values may be obtained by linear interpolation.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC)max. If the actual signal is always earlier than the nominal slew rate line between the shaded VREF(DC)-to-AC region, use the nominal slew rate for derating value (see Figure 21). If the actual signal is later than the nominal slew rate line anywhere between the shaded VREF(DC)-to-AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for derating value (see Figure 23).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VREF(DC). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between the shaded DC-to-VREF(DC) region, use the nominal slew rate for derating value (see Figure 22). If the actual signal is earlier than the nominal slew rate line anywhere between the shaded DC-to-VREF(DC) region, the slew rate of a tangent line to the actual signal from the DC level to the VREF(DC) level is used for derating value (see Figure 24).

Table 52 : Command and Address Setup and Hold Values Referenced – AC/DC-Based

Symbol	800	1066	1333	1600	1866	2133	Unit	Reference
^{t}IS(base, AC175)	200	125	65	45	–	–	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}IS(base, AC150)	350	275	190	170	–	–	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}IS(base, AC135)	–	–	–	–	65	60	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}IS(base, AC125)	–	–	–	–	150	135	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}IH(base, DC100)	275	200	140	120	100	95	ps	$V_{IH(DC)}/V_{IL(DC)}$

Table 53 : Derating Values for tIS/tIH – AC175/DC100-Based

Δ^{t}IS, Δ^{t}IH Derating (ps) – AC/DC-Based AC175 Threshold: $V_{IH(AC)} = V_{REF(DC)}$ + 175mV, $V_{IL(AC)} = V_{REF(DC)}$ - 175mV																
CMD/ ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IH	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH
2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	–2	–4	–2	–4	–2	–4	6	4	14	12	22	20	30	30	38	46
0.8	–6	–10	–6	–10	–6	–10	2	–2	10	6	18	14	26	24	34	40
0.7	–11	–16	–11	–16	–11	–16	–3	–8	5	0	13	8	21	18	29	34
0.6	–17	–26	–17	–26	–17	–26	–9	–18	–1	–10	7	–2	15	8	23	24
0.5	–35	–40	–35	–40	–35	–40	–27	–32	–19	–24	–11	–16	–2	–6	5	10
0.4	–62	–60	–62	–60	–62	–60	–54	–52	–46	–44	–38	–36	–30	–26	–22	–10

Table 54 : Derating Values for tIS/tIH – AC150/DC100-Based

Δ^{t}IS, Δ^{t}IH Derating (ps) – AC/DC-Based AC150 Threshold: $V_{IH(AC)} = V_{REF(DC)}$ + 150mV, $V_{IL(AC)} = V_{REF(DC)}$ - 150mV																
CMD/ ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IH	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH
2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	0	–4	0	–4	0	–4	8	4	16	12	24	20	32	30	40	46
0.8	0	–10	0	–10	0	–10	8	–2	16	6	24	14	32	24	40	40
0.7	0	–16	0	–16	0	–16	8	–8	16	0	24	8	32	18	40	34
0.6	–1	–26	–1	–26	–1	–26	7	–18	15	–10	23	–2	31	8	39	24
0.5	–10	–40	–10	–40	–10	–40	–2	–32	6	–24	14	–16	22	–6	30	10
0.4	–25	–60	–25	–60	–25	–60	–17	–52	–9	–44	–1	–36	7	–26	15	–10

Table 55 : Derating Values for tIS/tIH – AC135/DC100-Based

Δ^tIS, Δ^tIH Derating (ps) – AC/DC-Based AC135 Threshold: $V_{IH(AC)} = V_{REF(DC)} + 135mV$, $V_{IL(AC)} = V_{REF(DC)} - 135mV$																
CMD/ ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^tIS	Δ^tIH	Δ^tIS	Δ^tIH	Δ^tIS	Δ^tIH	Δ^tIS	Δ^tIH	Δ^tIS	Δ^tIH	Δ^tIH	Δ^tIH	Δ^tIS	Δ^tIH	Δ^tIS	Δ^tIH
2.0	68	50	68	50	68	50	76	58	84	66	92	74	100	84	108	100
1.5	45	34	45	34	45	34	53	42	61	50	69	58	77	68	85	84
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	2	–4	2	–4	2	–4	10	4	18	12	26	20	34	30	42	46
0.8	3	–10	3	–10	3	–10	11	–2	19	6	27	14	35	24	43	40
0.7	6	–16	6	–16	6	–16	14	–8	22	0	30	8	38	18	46	34
0.6	9	–26	9	–26	9	–26	17	–18	25	–10	33	–2	41	8	49	24
0.5	5	–40	5	–40	5	–40	13	–32	21	–24	29	–16	37	–6	45	10
0.4	–3	–60	–3	–60	–3	–60	6	–52	14	–44	22	–36	30	–26	38	–10

Table 56 : Derating Values for tIS/tIH – AC125/DC100-Based

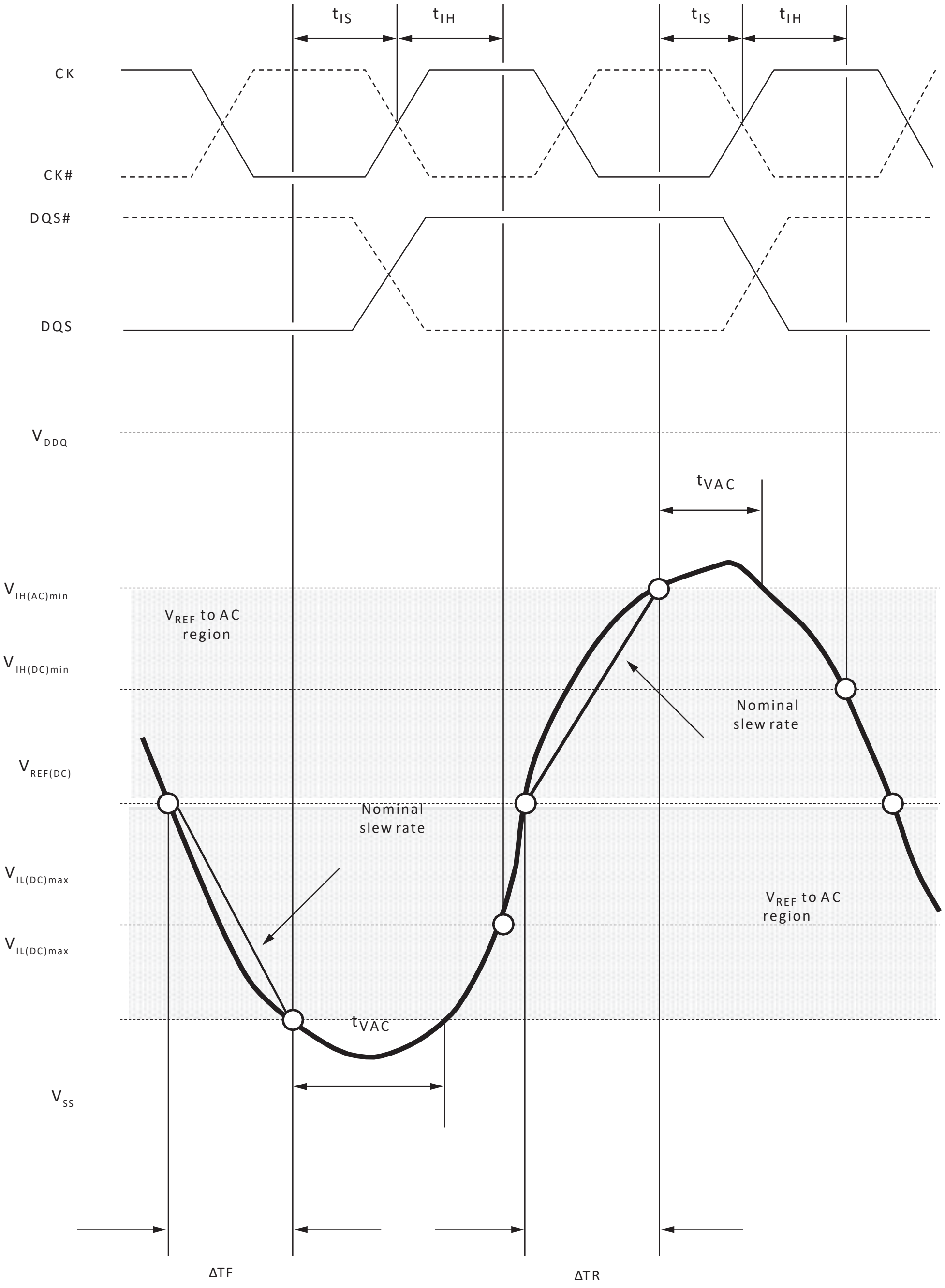
Δ^tIS, Δ^tIH Derating (ps) – AC/DC-Based AC125 Threshold: $V_{IH(AC)} = V_{REF(DC)} + 125mV$, $V_{IL(AC)} = V_{REF(DC)} - 125mV$																
CMD/ ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^tIS	Δ^tIH	Δ^tIS	Δ^tIH	Δ^tIS	Δ^tIH	Δ^tIS	Δ^tIH	Δ^tIS	Δ^tIH	Δ^tIH	Δ^tIH	Δ^tIS	Δ^tIH	Δ^tIS	Δ^tIH
2.0	63	50	63	50	63	50	71	58	79	66	87	74	95	84	103	100
1.5	42	34	42	34	42	34	50	42	58	50	66	58	74	68	82	84
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	4	–4	4	–4	4	–4	12	4	20	12	28	20	36	30	44	46
0.8	6	–10	6	–10	6	–10	14	–2	22	6	30	14	38	24	45	40
0.7	11	–16	11	–16	11	–16	19	–8	27	0	35	8	43	18	51	34
0.6	16	–26	16	–26	16	–26	24	–18	32	–10	40	–2	48	8	56	24
0.5	15	–40	15	–40	15	–40	23	–32	31	–24	39	–16	47	–6	55	10
0.4	13	–60	13	–60	13	–60	21	–52	29	–44	37	–36	45	–26	53	–10

Table 57 : Minimum Required Time tVAC Above VIH(AC) or Below VIL(AC)for Valid Transition

Slew Rate (V/ns)	^{t}VAC at 175mV (ps)	^{t}VAC at 150mV (ps)	^{t}VAC at 135mV (ps)	^{t}VAC at 125mV (ps)
>2.0	75	175	168	173
2.0	57	170	168	173
1.5	50	167	145	152
1.0	38	130	100	110
0.9	34	113	85	96
0.8	29	93	66	79
0.7	22	66	42	56
0.6	Note 1	30	10	27
0.5	Note 1	Note 1	Note 1	Note 1
<0.5	Note 1	Note 1	Note 1	Note 1

Note : 1. Rising input signal shall become equal to or greater than VIH(ac) level and Falling input signal shall become equal to or less than VIL(ac) level.

Figure 21 : Nominal Slew Rate and tVAC for tIS (Command and Address – Clock)

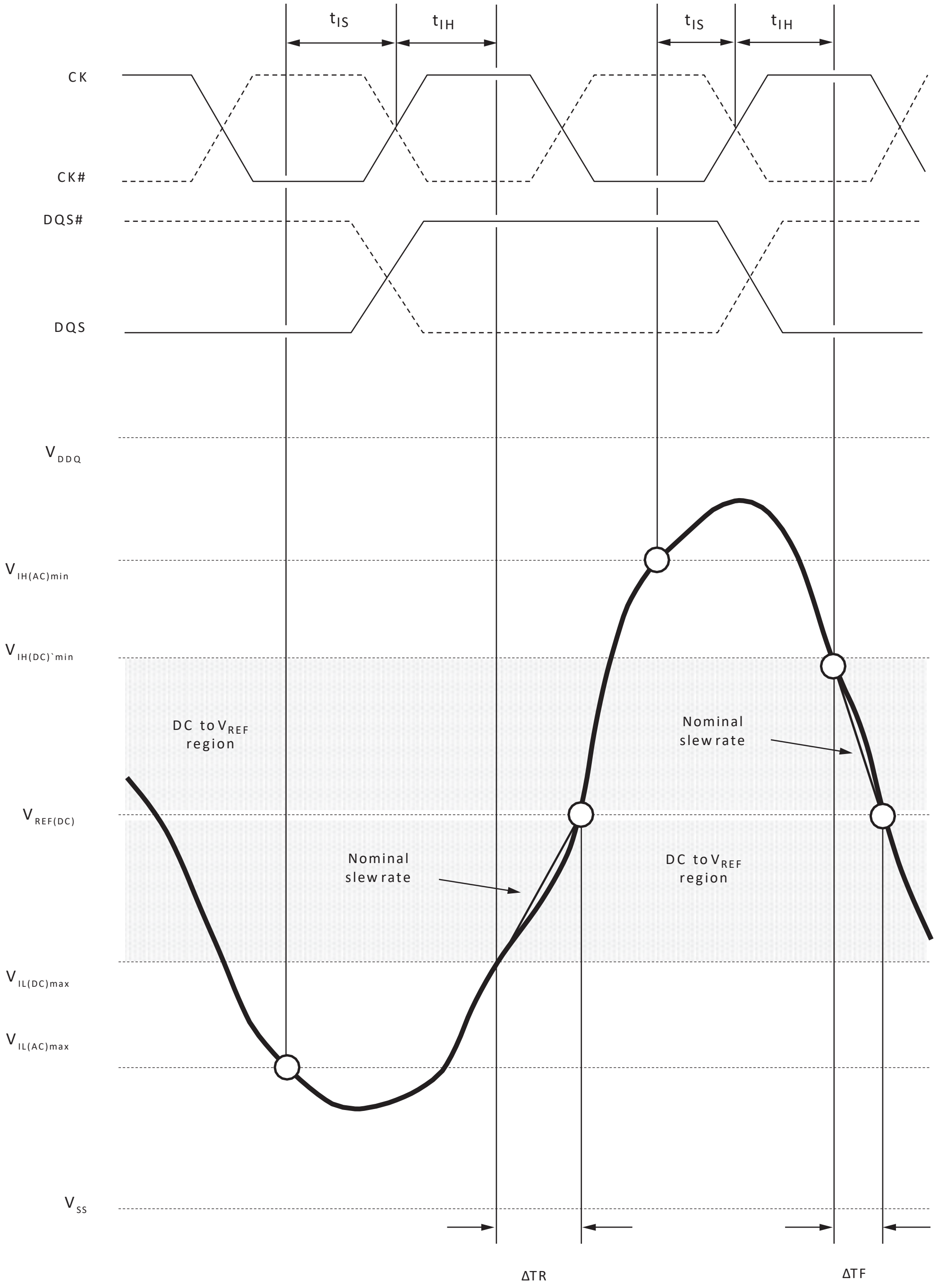


Setup slew rate falling signal $= \dfrac{V_{REF(DC)} - V_{IL(AC)max}}{\Delta TF}$

Setup slew rate rising signal $= \dfrac{V_{IH(AC)min} - V_{REF(DC)}}{\Delta TR}$

Note : 1. The clock and the strobe are drawn on different time scales.

Figure 22 : Nominal Slew Rate for tIH (Command and Address – Clock)

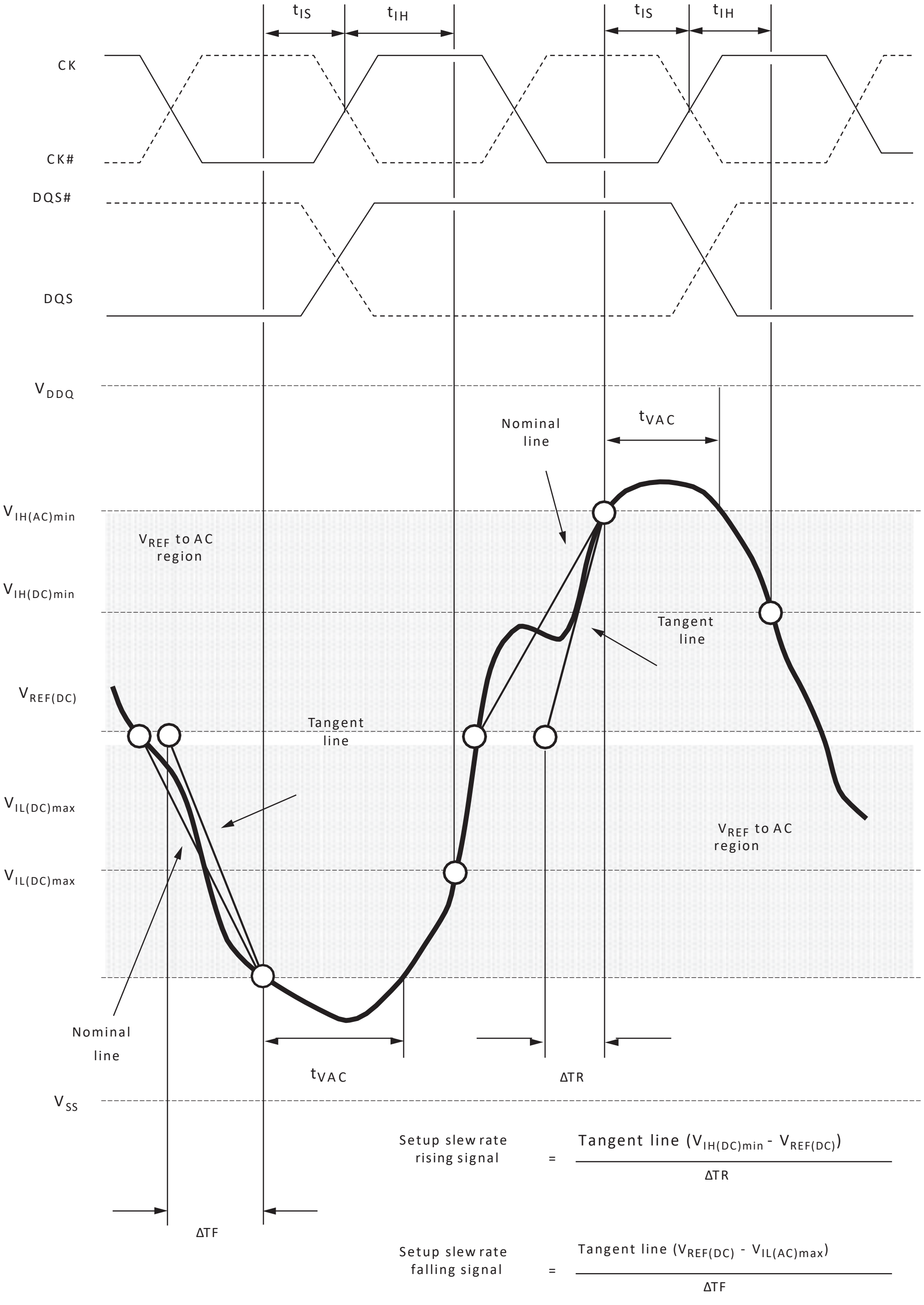


$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{V_{IH(DC)min} - V_{REF(DC)}}{\Delta TF}$$

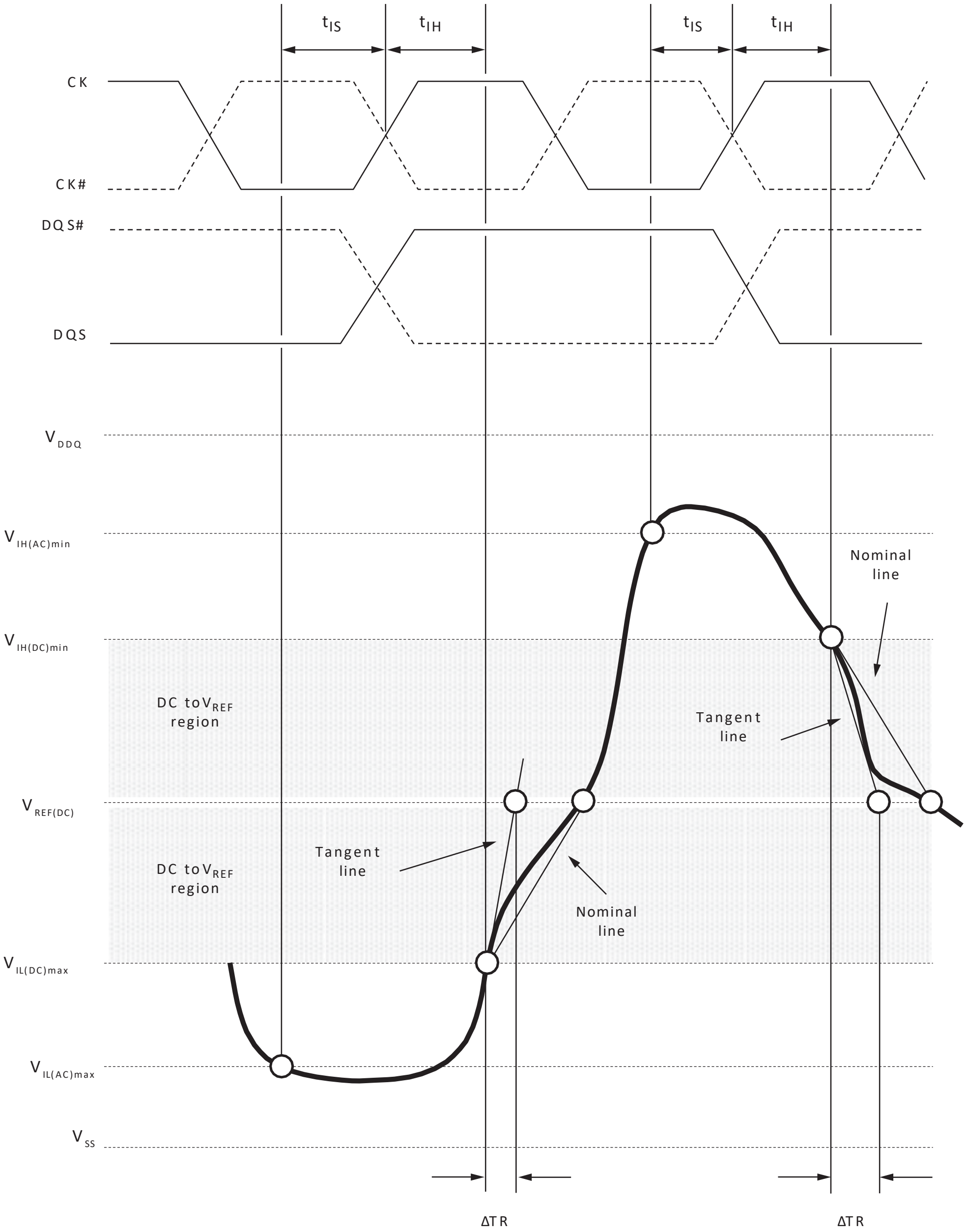
Note : 1. The clock and the strobe are drawn on different time scales.

Figure 23 : Tangent Line for tIS (Command and Address – Clock)



Note: 1. The clock and the strobe are drawn on different time scales.

Figure 24 : Tangent Line for tIH (Command and Address – Clock)



$$\text{Hold slew rate rising signal} = \frac{\text{Tangent line } (V_{REF(DC)} - V_{IL(DC)max})}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{\text{Tangent line } (V_{IH(DC)min} - V_{REF(DC)})}{\Delta TF}$$

Note : 1. The clock and the strobe are drawn on different time scales.

Data Setup, Hold, and Derating

The total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS (base) and tDH (base) values (see Table 58; values come from Table 01) to the ΔtDS and ΔtDH derating values (see Table 59), respectively. Example: tDS (total setup time) = tDS (base) + ΔtDS. For a valid transition, the input signal has to remain above/below VIH(AC)/VIL(AC) for some time tVAC (see Table 63).

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached VIH(AC)/VIL(AC)) at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach VIH/VIL(AC). For slew rates that fall between the values listed in Table 60, the derating values may obtained by linear interpolation.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC)max. If the actual signal is always earlier than the nominal slew rate line between the shaded VREF(DC)-to-AC region, use the nominal slew rate for derating value (see Figure 25). If the actual signal is later than the nominal slew rate line anywhere between the shaded VREF(DC)-to-AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for derating value (see Figure 27).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VREF(DC). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between the shaded DC-to-VREF(DC) region, use the nominal slew rate for derating value (see Figure 26). If the actual signal is earlier than the nominal slew rate line anywhere between the shaded DC-to-VREF(DC) region, the slew rate of a tangent line to the actual signal from the DC-to-VREF(DC) region is used for derating value (see Figure 28).

Table 58 : DDR3 Data Setup and Hold Values at 1 V/ns (DQS, DQS# at 2 V/ns) – AC/DC-Based

Symbol	800	1066	1333	1600	1866	2133	Unit	Reference
^{t}DS (base) AC175	75	25	–	–	–	–	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}DS (base) AC150	125	75	30	10	–	–	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}DS (base) AC135	165	115	60	40	68	53	ps	$V_{IH(AC)}/V_{IL(AC)}$
^{t}DH (base) DC100	150	100	65	45	70	55	ps	$V_{IH(DC)}/V_{IL(DC)}$
Slew Rate Referenced	1	1	1	1	2	2	V/ns	

Table 59 : Derating Values for tDS/tDH – AC175/DC100-Based

Shaded cells indicate slew rate combinations not supported

Δ^{t}DS, Δ^{t}DH Derating (ps) – AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH
2.0	88	50	88	50	88	50										
1.5	59	34	59	34	59	34	67	42								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			–2	–4	–2	–4	6	4	14	12	22	20				
0.8					–6	–10	2	–2	10	6	18	14	26	24		
0.7							–3	–8	5	0	13	8	21	18	29	34
0.6									–1	–10	7	–2	15	8	23	24
0.5											–11	–16	–2	–6	5	10
0.4													–30	–26	–22	–10

Table 60 : Derating Values for tDS/tDH – AC150/DC100-Based

Shaded cells indicate slew rate combinations not supported

Δ^tDS, Δ^tDH Derating (ps) – AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH
2.0	75	50	75	50	75	50										
1.5	50	34	50	34	50	34	58	42								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			0	–4	0	–4	8	4	16	12	24	20				
0.8					0	–10	8	–2	16	6	24	14	32	24		
0.7							8	–8	16	0	24	8	32	18	40	34
0.6									15	–10	23	–2	31	8	39	24
0.5											14	–16	22	–6	30	10
0.4													7	–26	15	–10

Table 61 : Derating Values for tDS/tDH – AC135/DC100-Based at 1V/ns

Shaded cells indicate slew rate combinations not supported

Δ^tDS, Δ^tDH Derating (ps) – AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH
2.0	68	50	68	50	68	50										
1.5	45	34	45	34	45	34	53	42								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			2	–4	2	–4	10	4	18	12	26	20				
0.8					3	–10	11	–2	19	6	27	14	35	24		
0.7							14	–8	22	0	30	8	38	18	46	34
0.6									25	–19	33	–2	41	8	49	24
0.5											29	–16	37	–6	45	–10
0.4													30	26	38	–10

Table 62 : Derating Values for tDS/tDH – AC135/DC100-Based at 2V/ns

Shaded cells indicate slew rate combinations not supported

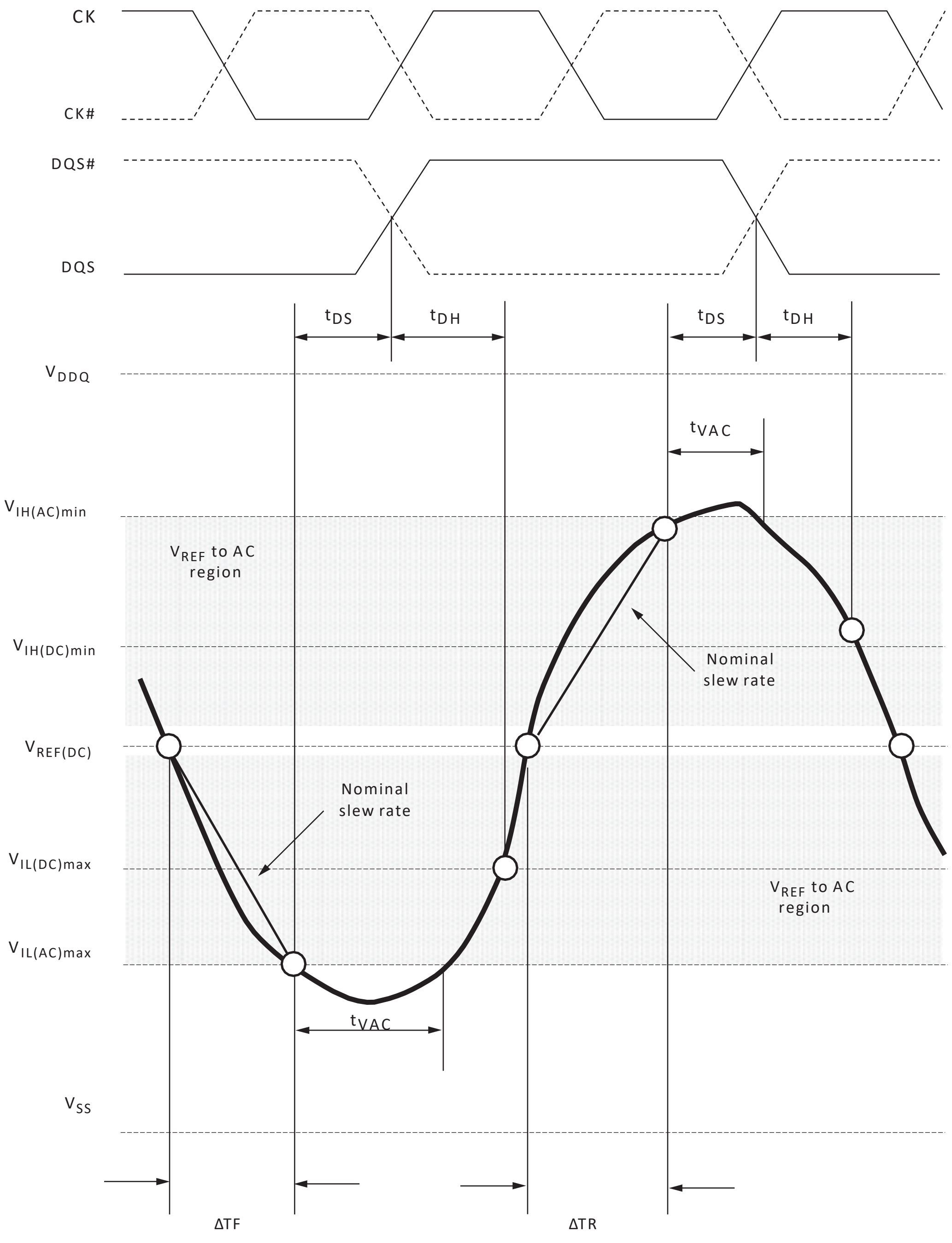
Δ^{t}DS, Δ^{t}DH Derating (ps) – AC/DC-Based																								
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate																							
	1.0 V/ns		1.2 V/ns		1.4 V/ns		1.6 V/ns		1.8 V/ns		2.0 V/ns		3.0 V/ns		4.0 V/ns		5.0 V/ns		6.0 V/ns		7.0 V/ns		8.0 V/ns	
	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS	Δ tDH	Δ tDS
4.0																			25	34	25	34	25	34
3.5																	21	29	21	29	21	29	21	29
3.0															17	23	17	23	17	23	17	23	17	23
2.5													10	14	10	14	10	14	10	14	10	14		
2.0											0	0	0	0	0	0	0	0	0	0				
1.5									–19	–15	–17	–23	–17	–23	–17	–23	–17	–23						
1.0							–34	–52	–42	–60	–50	–68	–50	–68	–50	–68								
0.9					–30	–42	–38	–50	–46	–58	–54	–66	–54	–66										
0.8			–26	–32	–36	–40	–40	–48	–52	–56	60	–64												
0.7	–17	–21	–33	–29	–43	–37	–51	–45	–59	–53														
0.6	–27	–19	–43	–27	–53	–35	–61	–43																
0.5	–40	–23	–56	–31	–66	–39																		
0.4	–60	–30	–76	–38																				

Table 63 : Required Minimum Time tVAC Above VIH(AC) (Below VIL(AC)) for Valid DQ Transition

Slew Rate (V/ns)	^{t}VAC at 175mV (ps)	^{t}VAC at 150mV (ps)	^{t}VAC at 135mV (ps)		
	DDR3-800/1066	DDR3-800/1066/1333/1600	DDR3-800/1066/1333/1600	DDR3-1866	DDR3-2133
>2.0	75	105	113	93	73
2.0	57	105	113	93	73
1.5	50	80	90	70	50
1.0	38	30	45	25	5
0.9	34	13	30	Note 1	Note 1
0.8	29	Note 1	11	Note 1	Note 1
0.7	Note 1	Note 1	Note 1	Note 1	Note 1
0.6	Note 1	Note 1	Note 1	Note 1	Note 1
0.5	Note 1	Note 1	Note 1	Note 1	Note 1
<0.5	Note 1	Note 1	Note 1	Note 1	Note 1

Note: 1. Rising input signal shall become equal to or greater than VIH(ac) level and Falling input signal shall become equal to or less than VIL(ac) level.

Figure 25 : Nominal Slew Rate and tVAC for tDS (DQ – Strobe)

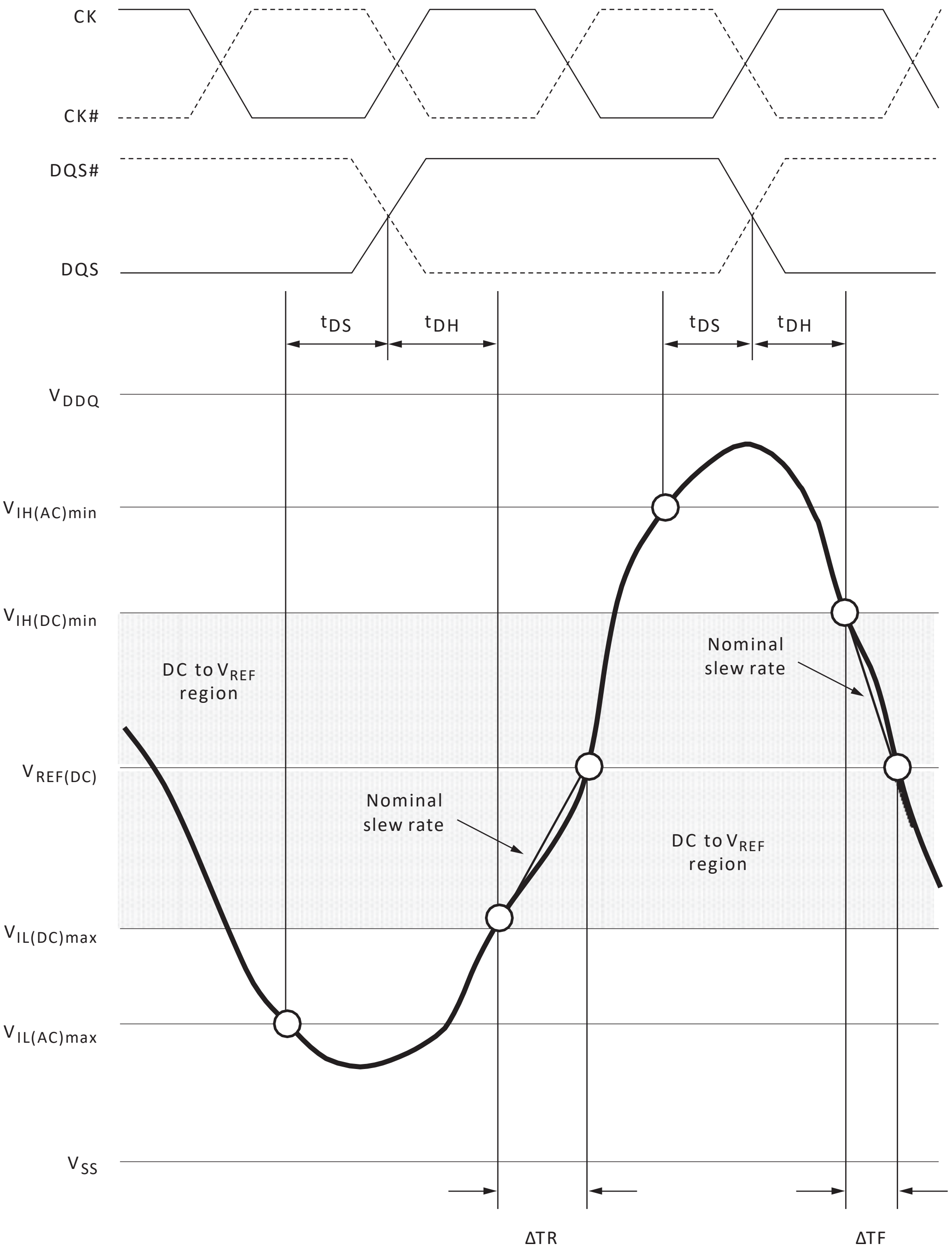


$$\text{Setup slew rate falling signal} = \frac{V_{REF(DC)} - V_{IL(AC)max}}{\Delta TF}$$

$$\text{Setup slew rate rising signal} = \frac{V_{IH(AC)min} - V_{REF(DC)}}{\Delta TR}$$

Note : 1. The clock and the strobe are drawn on different time scales.

Figure 26 : Nominal Slew Rate for tDH (DQ – Strobe)

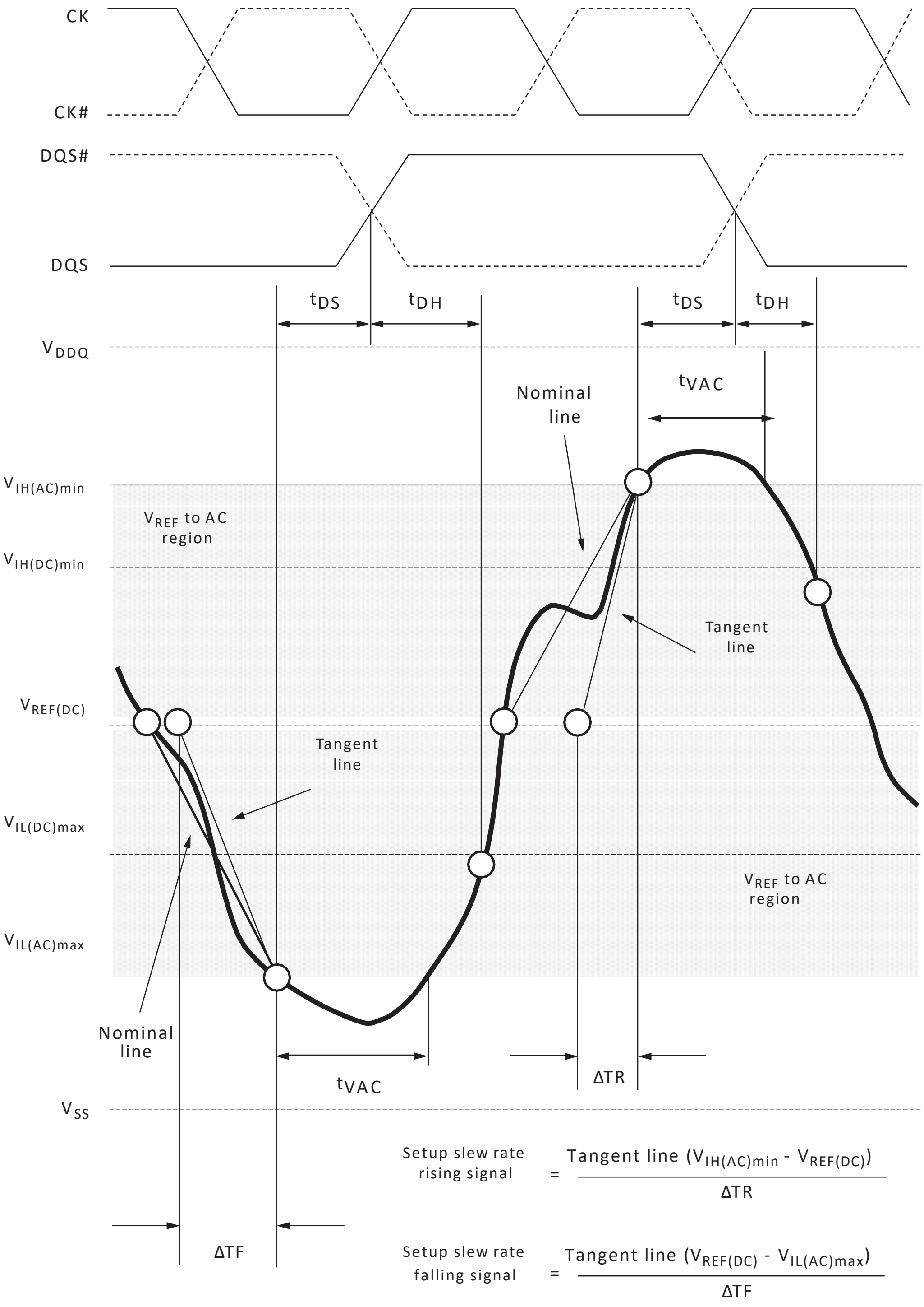


$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{V_{IL(DC)min} - V_{REF(DC)}}{\Delta TF}$$

Note : 1. The clock and the strobe are drawn on different time scales.

Figure 27 : Tangent Line for tDS (DQ – Strobe)

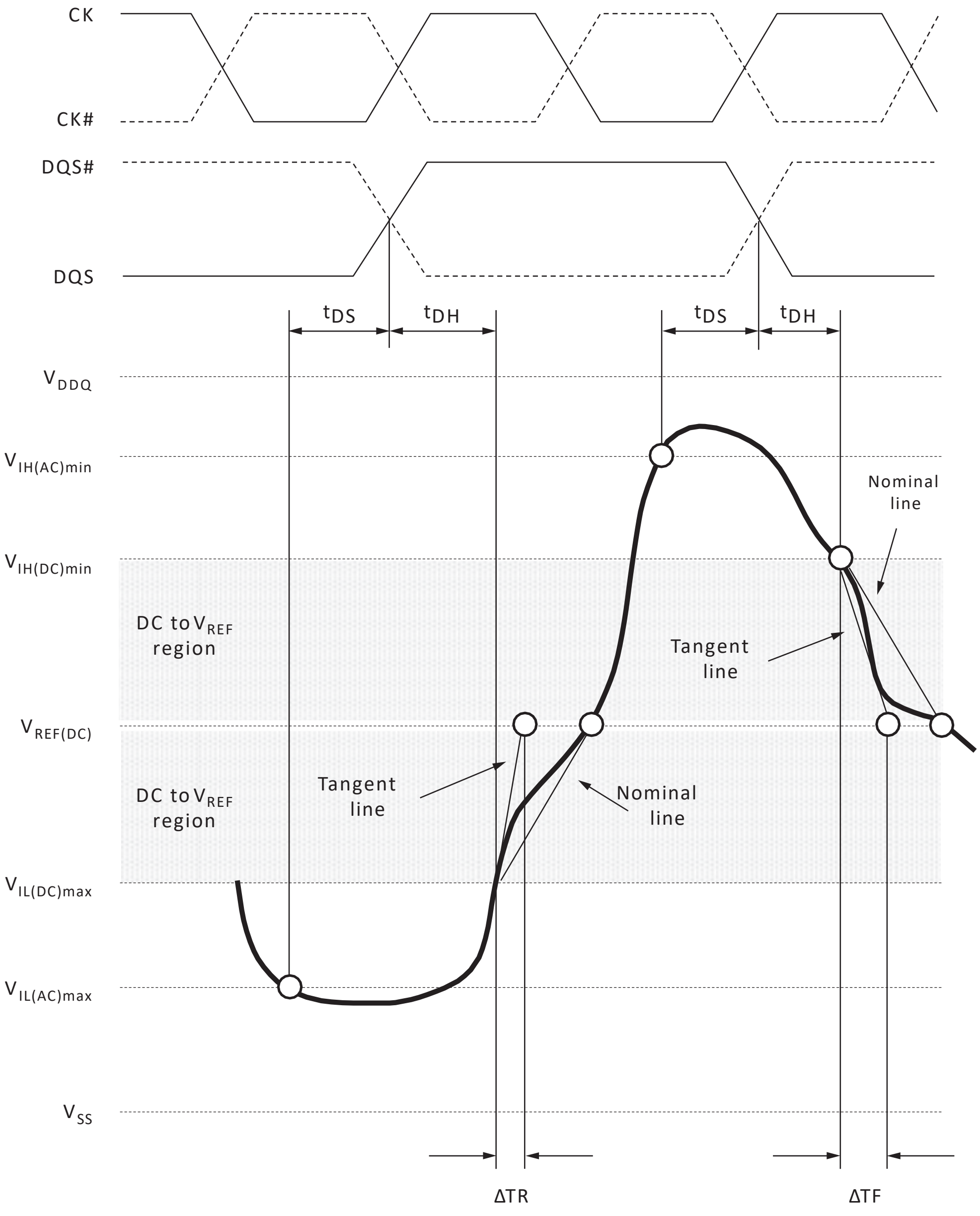


$$\text{Setup slew rate rising signal} = \frac{\text{Tangent line } (V_{IH(AC)min} - V_{REF(DC)})}{\Delta TR}$$

$$\text{Setup slew rate falling signal} = \frac{\text{Tangent line } (V_{REF(DC)} - V_{IL(AC)max})}{\Delta TF}$$

Note : 1. The clock and the strobe are drawn on different time scales.

Figure 28 : Tangent Line for tDH (DQ – Strobe)



$$\text{Hold slew rate rising signal} = \frac{\text{Tangent line } (V_{REF(DC)} - V_{IL(DC)max})}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{\text{Tangent line } (V_{IH(DC)min} - V_{REF(DC)})}{\Delta TF}$$

Note: 1. The clock and the strobe are drawn on different time scales.

Commands – Truth Tables

Table 64 : Truth Table – Command

Notes 1–5 apply to the entire table

Function		Symbol	CKE		CS#	RAS#	CAS#	WE#	BA [2:0]	A*n*	A12	A10	A[11, 9:0]	Notes
			Prev. Cycle	Next Cycle										
MODE REGISTER SET		MRS	H	H	L	L	L	L	BA	OP code				
REFRESH		REF	H	H	L	L	L	H	V	V	V	V	V	
Self refresh entry		SRE	H	L	L	L	L	H	V	V	V	V	V	6
Self refresh exit		SRX	L	H	H	V	V	V	V	V	V	V	V	6.7
					L	H	H	H						
Single-bank PRECHARGE		PRE	H	H	L	L	H	L	BA	V	V	L	V	
PRECHARGE all banks		PREA	H	H	L	L	H	L	V		V	H	V	
Bank ACTIVATE		ACT	H	H	L	L	H	H	BA	Row address (RA)				
WRITE	BL8MRS, BC4MRS	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	8
	BC4OTF	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	8
	BL8OTF	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	8
WRITE with auto precharge	BL8MRS, BC4MRS	WRAP	H	H	L	H	L	L	BA	RFU	V	H	CA	8
	BC4OTF	WRAPS4	H	H	L	H	L	L	BA	RFU	L	H	CA	8
	BL8OTF	WRAPS8	H	H	L	H	L	L	BA	RFU	H	H	CA	8
READ	BL8MRS, BC4MRS	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	8
	BC4OTF	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	8
	BL8OTF	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	8
READ with auto precharge	BL8MRS, BC4MRS	RDAP	H	H	L	H	L	H	BA	RFU	V	H	CA	8
	BC4OTF	RDAPS4	H	H	L	H	L	H	BA	RFU	L	H	CA	8
	BL8OTF	RDAPS8	H	H	L	H	L	H	BA	RFU	H	H	CA	8
NO OPERATION		NOP	H	H		H	H	H	V	V	V	V	V	9
Device DESELECTED		DES	H	H	H	X	X	X	X	X	X	X	X	10
Power-down entry		PDE	H	L	L	H	H	H	V	V	V	V	V	6
					H	V	V	V						
Power-down exit		PDX	L	H	L	H	H	H	V	V	V	V	V	6,11
					H	V	V	V						
ZQ CALIBRATION LONG		ZQCL	H	H	L	H	H	L	X	X	X	H	X	12
ZQ CALIBRATION SHORT		ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Notes :

1. Commands are defined by the states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device-, density-, and configuration dependent.
2. RESET# is enabled LOW and used only for asynchronous reset. Thus, RESET# must be held HIGH during any normal operation.
3. The state of ODT does not affect the states described in this table.
4. Operations apply to the bank defined by the bank address. For MRS, BA selects one of four mode registers.
5. “V” means “H” or “L” (a defined logic level), and “X” means “Don’t Care.”
6. See Table 65 for additional information on CKE transition.
7. Self refresh exit is asynchronous.
8. Burst READs or WRITEs cannot be terminated or interrupted. MRS (fixed) and OTF BL/BC are defined in MR0.
9. The purpose of the NOP command is to prevent the DRAM from registering any unwanted commands. A NOP will not terminate an operation that is executing.
10. The DES and NOP commands perform similarly.
11. The power-down mode does not perform any REFRESH operations.
12. ZQ CALIBRATION LONG is used for either ZQinit (first ZQCL command during initialization) or ZQoper (ZQCL command after initialization).

Table 65 : Truth Table – CKE

Notes 1–2 apply to the entire table; see Table 64 for additional command details

Current State[3]	CKE		Command[5] (RAS#, CAS#, WE#, CS#)	Action[5]	Notes
	Previous Cycle[4] (*n* - 1)	Present Cycle[4] (*n*)			
Power-down	L	L	“Don’t Care”	Maintain power-down	
	L	H	DES or NOP	Power-down exit	
Self refresh	L	L	“Don’t Care”	Maintain self refresh	
	L	H	DES or NOP	Self refresh exit	
Bank(s) active	H	L	DES or NOP	Active power-down entry	
Reading	H	L	DES or NOP	Power-down entry	
Writing	H	L	DES or NOP	Power-down entry	
Precharging	H	L	DES or NOP	Power-down entry	
Refreshing	H	L	DES or NOP	Precharge power-down entry	
All banks idle	H	L	DES or NOP	Precharge power-down entry	6
	H	L	REFRESH	Self refresh	

Notes :
1. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
2. tCKE (MIN) means CKE must be registered at multiple consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the required number of registration clocks. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKE (MIN) + tIH.
3. Current state = The state of the DRAM immediately prior to clock edge *n*.
4. CKE (*n*) is the logic state of CKE at clock edge *n*; CKE (*n* - 1) was the state of CKE at the previous clock edge.
5. COMMAND is the command registered at the clock edge (must be a legal command as defined in Table 64. Action is a result of COMMAND. ODT does not affect the states described in this table and is not listed.
6. Idle state = All banks are closed, no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied. All self refresh exit and power-down exit parameters are also satisfied.

Commands

DESELECT

The DESELECT (DES) command (CS# HIGH) prevents new commands from being executed by the DRAM. Operations already in progress are not affected.

NO OPERATION

The NO OPERATION (NOP) command (CS# LOW) prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

ZQ CALIBRATION LONG

The ZQ CALIBRATION LONG (ZQCL) command is used to perform the initial calibration during a power-up initialization and reset sequence (see Figure 37). This command may be issued at any time by the controller, depending on the system environment. The ZQCL command triggers the calibration engine inside the DRAM. After calibration is achieved, the calibrated values are transferred from the calibration engine to the DRAM I/O, which are reflected as updated RON and ODT values. The DRAM is allowed a timing window defined by either tZQinit or tZQoper to perform a full calibration and transfer of values. When ZQCL is issued during the initialization sequence, the timing parameter tZQinit must be satisfied. When initialization is complete, subsequent ZQCL commands require the timing parameter tZQoper to be satisfied.

ZQ CALIBRATION SHORT

The ZQ CALIBRATION SHORT (ZQCS) command is used to perform periodic calibrations to account for small voltage and temperature variations. A shorter timing window is provided to perform the reduced calibration and transfer of values as defined by timing parameter tZQCS. A ZQCS command can effectively correct a minimum of 0.5% RON and RTT impedance error within 64 clock cycles, assuming the maximum sensitivities specified in Table 36 and Table 37.

ACTIVATE

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA[2:0] inputs selects the bank, and the address provided on inputs A[*n*:0] selects the row. This row remains open (or active) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The address provided on inputs A[2:0] selects the starting column address, depending on the burst length and burst type selected (see Burst Order table for additional information). The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst. If auto precharge is not selected, the row will remain open for subsequent accesses. The value on input A12 (if enabled in the mode register) when the READ command is issued determines whether BC4 (chop) or BL8 is used. After a READ command is issued, the READ burst may not be interrupted.

Table 66 : READ Command Summary

Function		Symbol	CKE		CS#	RAS#	CAS#	WE#	BA [2:0]	A*n*	A12	A10	A[11, 9:0]
			Prev. Cycle	Next Cycle									
READ	BL8MRS, BC4MRS	RD	H		L	H	L	H	BA	RFU	V	L	CA
	BC4OTF	RDS4	H		L	H	L	H	BA	RFU	L	L	CA
	BL8OTF	RDS8	H		L	H	L	H	BA	RFU	H	L	CA
READ with auto precharge	BL8MRS, BC4MRS	RDAP	H		L	H	L	H	BA	RFU	V	H	CA
	BC4OTF	RDAPS4	H		L	H	L	H	BA	RFU	L	H	CA
	BL8OTF	RDAPS8	H		L	H	L	H	BA	RFU	H	H	CA

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA[2:0] inputs selects the bank. The value on input A10 determines whether auto precharge is used. The value on input A12 (if enabled in the MR) when the WRITE command is issued determines whether BC4 (chop) or BL8 is used.

Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored and a WRITE will not be executed to that byte/column location..

Table 67 : WRITE Command Summary

Function		Symbol	CKE		CS#	RAS#	CAS#	WE#	BA [2:0]	A*n*	A12	A10	A[11, 9:0]
			Prev. Cycle	Next Cycle									
WRITE	BL8MRS BC4MR	WR	H		L	H	L	L	BA	RFU	V	L	CA
	BC4OTF	WRS4	H		L	H	L	L	BA	RFU	L	L	CA
	BL8OTF	WRS8	H		L	H	L	L	BA	RFU	H	L	CA
WRITE with auto precharge	BL8MRS BC4MRS	WRAP	H		L	H	L	L	BA	RFU	V	H	CA
	BC4OTF	WRAPS4	H		L	H	L	L	BA	RFU	L	H	CA
	BL8OTF	WRAPS8	H		L	H	L	L	BA	RFU	H	H	CA

PRECHARGE

The PRECHARGE command is used to de-activate the open row in a particular bank or in all banks. The bank(s) are available for a subsequent row access a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge.

A READ or WRITE command to a different bank is allowed during a concurrent auto precharge as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are precharged. In the case where only one bank is precharged, inputs BA[2:0] select the bank; otherwise, BA[2:0] are treated as “Don’t Care.”

After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is treated as a NOP if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period is determined by the last PRECHARGE command issued to the bank.

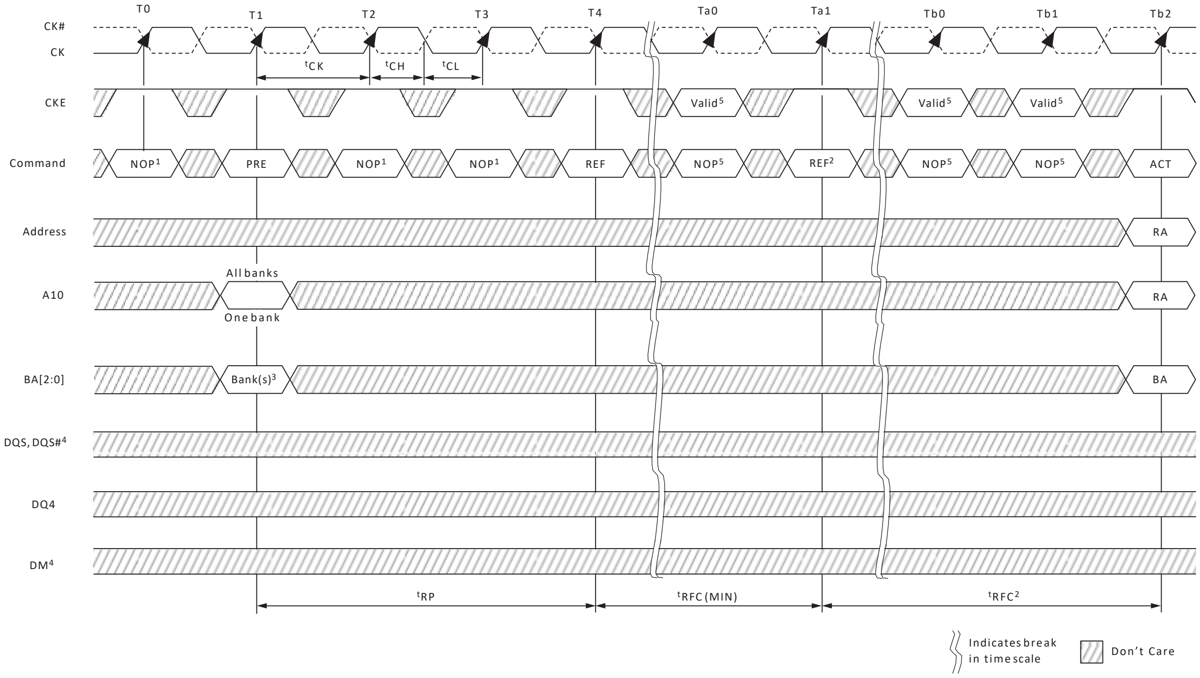
REFRESH

The REFRESH command is used during normal operation of the DRAM and is analogous to CAS#-before-RAS# (CBR) refresh or auto refresh. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a “Don’t Care” during a REFRESH command.

The DRAM requires REFRESH cycles at an average interval of 7.8µs (maximum when TC ≤ 85°C or 3.9µs maximum when TC ≤ 95°C). The REFRESH period begins when the REFRESH command is registered and ends tRFC (MIN) later. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be posted to any given DRAM, meaning that the maximum absolute interval between any REFRESH command and the next REFRESH command is nine times the maximum average interval refresh rate. Self refresh may be entered with up to eight REFRESH commands being posted. After exiting self refresh (when entered with posted REFRESH commands), additional posting of REFRESH commands is allowed to the extent that the maximum number of cumulative posted REFRESH commands (both preand post-self refresh) does not exceed eight REFRESH commands.

At any given time, a maximum of 16 REFRESH commands can be issued within 2 x tREFI.

Figure 29 : Refresh Mode



Notes :
1. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during the PRECHARGE, ACTIVATE, and REFRESH commands, but may be inactive at other times (see Power-Down Mode).
2. The second REFRESH is not required, but two back-to-back REFRESH commands are shown.
3. "Don't Care" if A10 is HIGH at this point; however, A10 must be HIGH if more than one bank is active(must precharge all active banks).
4. For operations shown, DM, DQ, and DQS signals are all "Don't Care"/High-Z.
5. Only NOP and DES commands are allowed after a REFRESH command and until tRFC (MIN) is satisfied.

SELF REFRESH

The SELF REFRESH command is used to retain data in the DRAM, even if the rest of the system is powered down. When in self refresh mode, the DRAM retains data without external clocking. Self refresh mode is also a convenient method used to enable/disable the DLL as well as to change the clock frequency within the allowed synchronous operating range (see Input Clock Frequency Change). All power supply inputs (including VREFCA and VREFDQ) must be maintained at valid levels upon entry/exit and during self refresh mode operation. VREFDQ may float or not drive VDDQ/2 while in self refresh mode under the following conditions:

- VSS < VREFDQ < VDD is maintained
- VREFDQ is valid and stable prior to CKE going back HIGH
- The first WRITE operation may not occur earlier than 512 clocks after VREFDQ is valid
- All other self refresh mode exit timing requirements are met

DLL Disable Mode

If the DLL is disabled by the mode register (MR1[0] can be switched during initialization or later), the DRAM is targeted, but not guaranteed, to operate similarly to the normal mode, with a few notable exceptions:

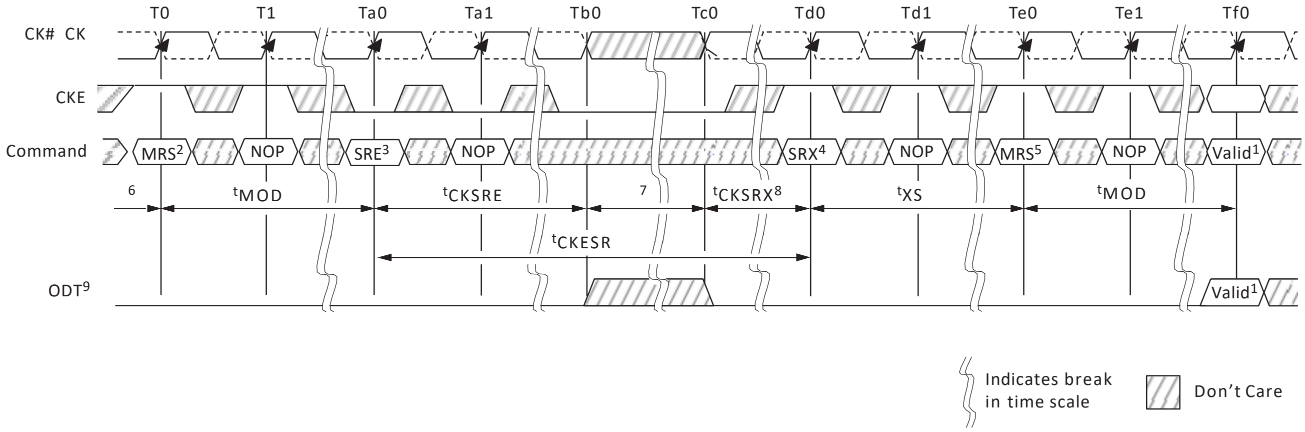
- The DRAM supports only one value of CAS latency (CL=6) and one value of CAS WRITE latency (CWL=6).
- DLL disable mode affects the read data clock-to-data strobe relationship (tDQSCK), but not the read data-to-data strobe relationship (tDQSQ, tQH). Special attention is required to line up the read data with the controller time domain when the DLL is disabled.
- In normal operation (DLL on), tDQSCK starts from the rising clock edge AL + CL cycles after the READ command. In DLL disable mode, tDQSCK starts AL + CL - 1 cycles after the READ command. Additionally, with the DLL disabled, the value of tDQSCK could be larger than tCK.

The ODT feature (including dynamic ODT) is not supported during DLL disable mode. The ODT resistors must be disabled by continuously registering the ODT ball LOW by programming RTT,nom MR1[9, 6, 2] and RTT (WR) MR2[10, 9] to 0 while in the DLL disable mode.

Specific steps must be followed to switch between the DLL enable and DLL disable modes due to a gap in the allowed clock rates between the two modes (tCK [AVG] MAX and tCK [DLL_DIS] MIN, respectively). The only time the clock is allowed to cross this clock rate gap is during self refresh mode. Thus, the required procedure for switching from the DLL enable mode to the DLL disable mode is to change frequency during self refresh:

1. Starting from the idle state (all banks are precharged, all timings are fulfilled, ODT is turned off, and $R_{TT,nom}$ and $R_{TT(WR)}$ are High-Z, set MR1[0] to 1 to disable the DLL.
2. Enter self refresh mode after tMOD has been satisfied.
3. After tCKSRE is satisfied, change the frequency to the desired clock rate.
4. Self refresh may be exited when the clock is stable with the new frequency for tCKSRX. After tXS is satisfied, update the mode registers with appropriate values.
5. The DRAM will be ready for its next command in the DLL disable mode after the greater of tMRD or tMOD has been satisfied. A ZQCL command should be issued with appropriate timings met.

Figure 30 : DLL Enable Mode to DLL Disable Mode

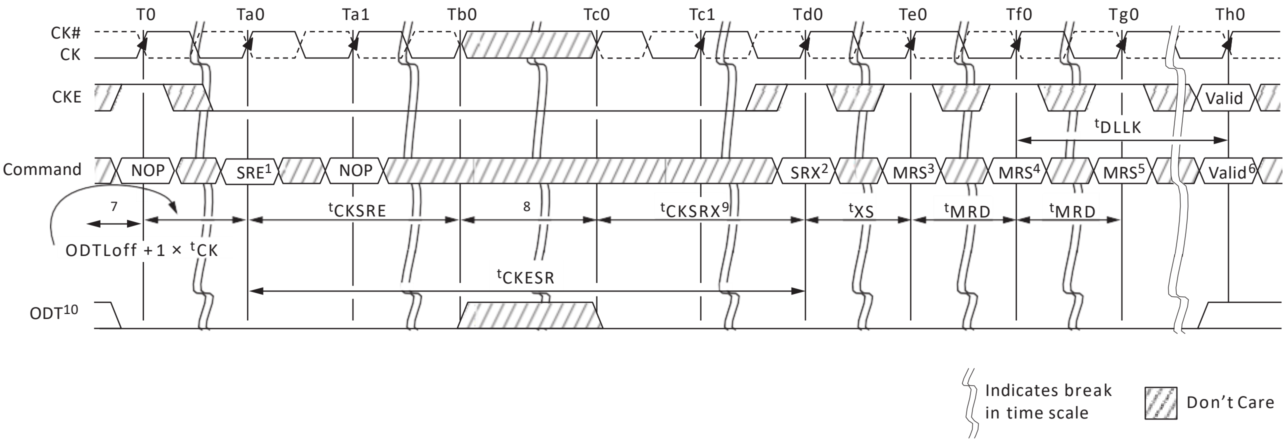


Notes :
1. Any valid command.
2. Disable DLL by setting MR1[0] to 1.
3. Enter SELF REFRESH.
4. Exit SELF REFRESH.
5. Update the mode registers with the DLL disable parameters setting.
6. Starting with the idle state, RTT is in the High-Z state.
7. Change frequency.
8. Clock must be stable tCKSRX.
9. Static LOW in the case that RTT,nom or RTT(WR) is enabled; otherwise, static LOW or HIGH.

A similar procedure is required for switching from the DLL disable mode back to the DLL enable mode. This also requires changing the frequency during self refresh mode (see Figure 31).

1. Starting from the idle state (all banks are precharged, all timings are fulfilled, ODT is turned off, and RTT,nom and RTT(WR) are High-Z), enter self refresh mode.
2. After tCKSRE is satisfied, change the frequency to the new clock rate.
3. Self refresh may be exited when the clock is stable with the new frequency for tCKSRX. After tXS is satisfied, update the mode registers with the appropriate values. At a minimum, set MR1[0] to 0 to enable the DLL. Wait tMRD, then set MR0[8] to 1 to enable DLL RESET.
4. After another tMRD delay is satisfied, update the remaining mode registers with the appropriate values.
5. The DRAM will be ready for its next command in the DLL enable mode after the greater of tMRD or tMOD has been satisfied. However, before applying any command or function requiring a locked DLL, a delay of tDLLK after DLL RESET must be satisfied. A ZQCL command should be issued with the appropriate timings met.

Figure 31 : DLL Disable Mode to DLL Enable Mode



Notes :
1. Enter SELF REFRESH.
2. Exit SELF REFRESH.
3. Wait tXS, then set MR1[0] to 0 to enable DLL.
4. Wait tMRD, then set MR0[8] to 1 to begin DLL RESET.
5. Wait tMRD, update registers (CL, CWL, and write recovery may be necessary).
6. Wait tMOD, any valid command.
7. Starting with the idle state.
8. Change frequency.
9. Clock must be stable at least tCKSRX.
10. Static LOW in the case that RTT,nom or RTT(WR) is enabled; otherwise, static LOW or HIGH.

The clock frequency range for the DLL disable mode is specified by the parameter tCK (DLL_DIS). Due to latency counter and timing restrictions, only CL = 6 and CWL = 6 are supported.

DLL disable mode will affect the read data clock to data strobe relationship (tDQSCK) but not the data strobe to data relationship (tDQSQ, tQH). Special attention is needed to line up read data to the controller time domain.

Compared to the DLL on mode where tDQSCK starts from the rising clock edge AL + CL cycles after the READ command, the DLL disable mode tDQSCK starts AL + CL - 1 cycles after the READ command.

WRITE operations function similarly between the DLL enable and DLL disable modes; however, ODT functionality is not allowed with DLL disable mode.

Figure 32 : DLL Disable tDQSCK

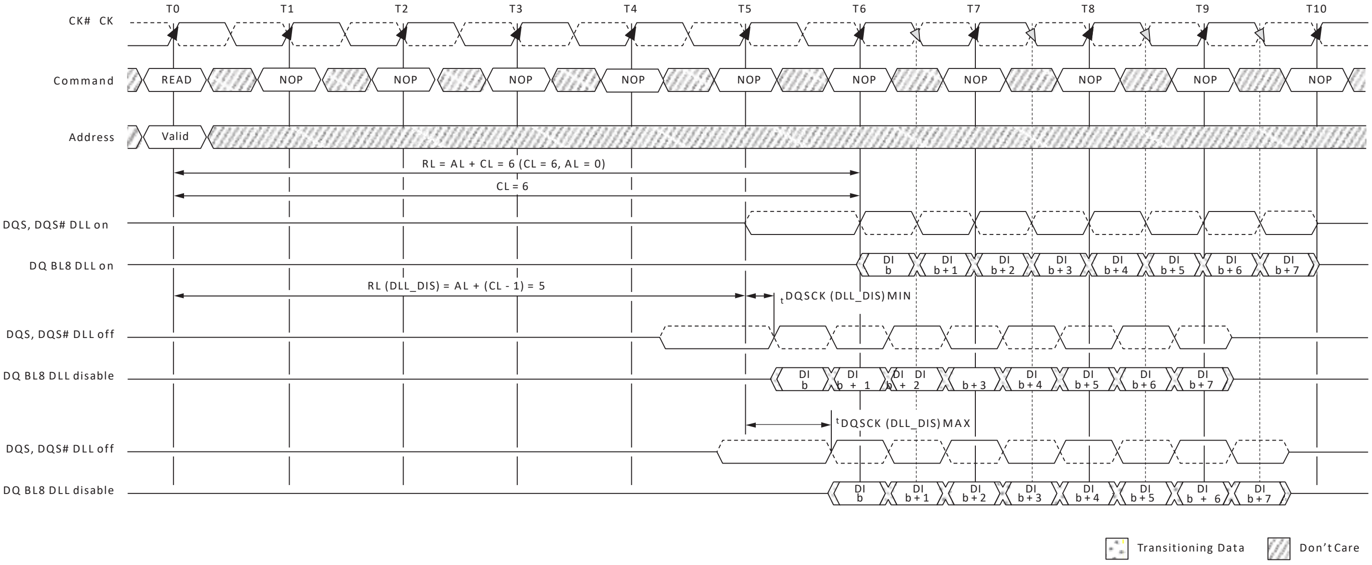


Table 68 : READ Electrical Characteristics, DLL Disable Mode

Parameter	Symbol	Min	Max	Unit
Access window of DQS from CK, CK#	^{t}DQSCK (DLL_DIS)	1	10	ns

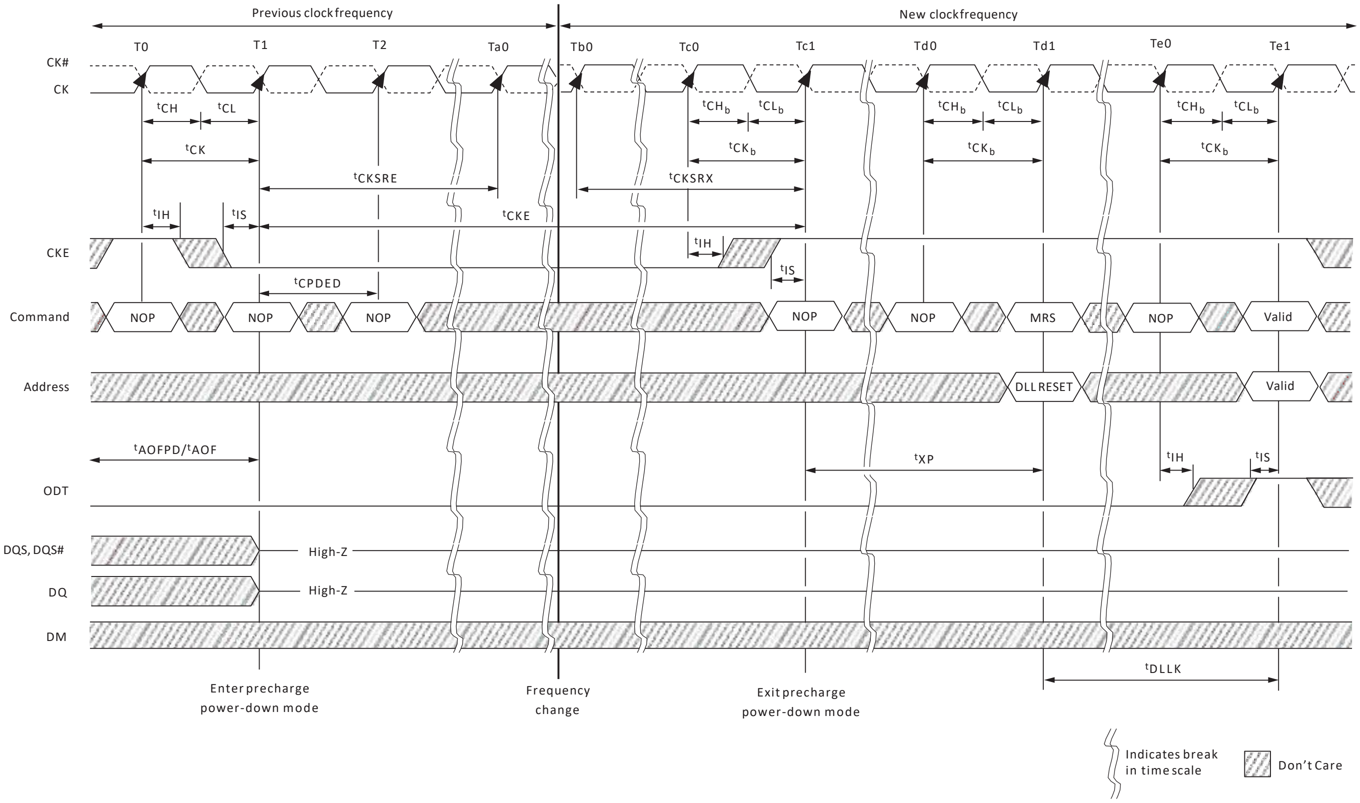
Input Clock Frequency Change

When the DDR3 SDRAM is initialized, the clock must be stable during most normal states of operation. This means that after the clock frequency has been set to the stable state, the clock period is not allowed to deviate, except for hat is allowed by the clock jitter and spread spectrum clocking (SSC) specifications.

The input clock frequency can be changed from one stable clock rate to another under two conditions: self refresh mode and precharge power-down mode. It is illegal to change the clock frequency outside of those two modes. For the self refresh mode condition, when the DDR3 SDRAM has been successfully placed into self refresh mode and tCKSRE has been satisfied, the state of the clock becomes a “Don’t Care.” When the clock becomes a “Don’t Care,” changing the clock frequency is permissible if the new clock frequency is stable prior to tCKSRX. When entering and exiting self refresh mode for the sole purpose of changing the clock frequency, the self refresh entry and exit specifications must still be met.

The precharge power-down mode condition is when the DDR3 SDRAM is in precharge power-down mode (either fast exit mode or slow exit mode). Either ODT must be at a logic LOW or RTT,nom and RTT(WR) must be disabled via MR1 and MR2. This ensures RTT,nom and RTT(WR) are in an off state prior to entering precharge power-down mode, and CKE must be at a logic LOW. A minimum of tCKSRE must occur after CKE goes LOW before the clock frequency can change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade (tCK [AVG] MIN to tCK [AVG] MAX). During the input clock frequency change, CKE must be held at a stable LOW level. When the input clock frequency is changed, a stable clock must be provided to the DRAM tCKSRX before precharge power-down may be exited. After precharge power-down is exited and tXP has been satisfied, the DLL must be reset via the MRS. Depending on the new clock frequency, additional MRS commands may need to be issued. During the DLL lock time, RTT,nom and RTT(WR) must remain in an off state. After the DLL lock time, the DRAM is ready to operate with a new clock frequency.

Figure 33 : Change Frequency During Precharge Power-Down



Notes : 1. Applicable for both SLOW-EXIT and FAST-EXIT precharge power-down modes.

2. tAOFPD and tAOF must be satisfied and outputs High-Z prior to T1 (see On-Die Termination (ODT)) for exact requirements).

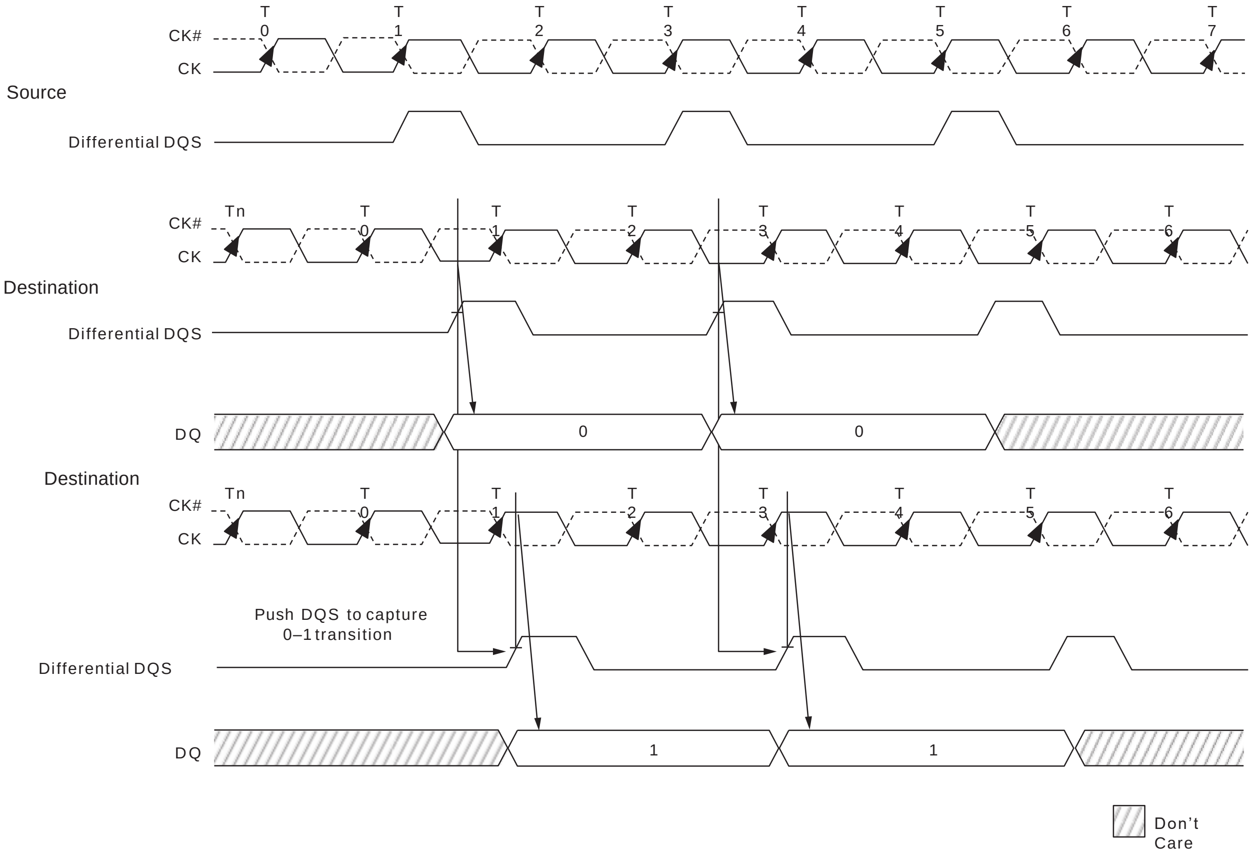
3. If the RTT,nom feature was enabled in the mode register prior to entering precharge power-down mode, the ODT signal must be continuously registered LOW, ensuring RTT is in an off state. If the RTT,nom feature was disabled in the mode register prior to entering precharge power-down mode, RTT will remain in the off state. The ODT signal can be registered LOW or HIGH in this case.

Write Leveling

For better signal integrity, DDR3 SDRAM memory modules have adopted fly-by topology for the commands, addresses, control signals, and clocks. Write leveling is a scheme for the memory controller to adjust or de-skew the DQS strobe (DQS, DQS#) to CK relationship at the DRAM with a simple feedback feature provided by the DRAM. Write leveling is generally used as part of the initialization process, if required. For normal DRAM operation, this feature must be disabled. This is the only DRAM operation where the DQS functions as an input (to capture the incoming clock) and the DQ function as outputs (to report the state of the clock). Note that nonstandard ODT schemes are required.

The memory controller using the write leveling procedure must have adjustable delay settings on its DQS strobe to align the rising edge of DQS to the clock at the DRAM pins. This is accomplished when the DRAM asynchronously feeds back the CK status via the DQ bus and samples with the rising edge of DQS. The controller repeatedly delays the DQS strobe until a CK transition from 0 to 1 is detected. The DQS delay established by this procedure helps ensure tDQSS, tDSS, and tDSH specifications in systems that use fly-by topology by de-skewing the trace length mismatch. A conceptual timing of this procedure is shown in Figure 34.

Figure 34 : Write Leveling Concept



When write leveling is enabled, the rising edge of DQS samples CK, and the prime DQ outputs the sampled CK's status. The prime DQ for a x4 or x8 configuration is DQ0 with all other DQ (DQ[7:1]) driving LOW. The prime DQ for a x16 configuration is DQ0 for the lower byte and DQ8 for the upper byte. It outputs the status of CK sampled by LDQS and UDQS. All other DQ (DQ[7:1], DQ[15:9]) continue to drive LOW. Two prime DQ on a x16 enable each byte lane to be leveled independently.

The write leveling mode register interacts with other mode registers to correctly configure the write leveling functionality. Besides using MR1[7] to disable/enable write leveling, MR1[12] must be used to enable/disable the output buffers. The ODT value, burst length, and so forth need to be selected as well. This interaction is shown in Table 69. It should also be noted that when the outputs are enabled during write leveling mode, the DQS buffers are set as inputs, and the DQ are set as outputs. Additionally, during write leveling mode, only the DQS strobe terminations are activated and deactivated via the ODT ball. The DQ remain disabled and are not affected by the ODT ball.

Table 69 : Write Leveling Matrix

Note 1 applies to the entire table

MR1[7]	MR1[12]	MR1[2, 6, 9]	DRAM ODT Ball	DRAM $R_{TT,nom}$		DRAM State	Case	Notes
Write Leveling	Output Buffers	$R_{TT,nom}$ Value		DQS	DQ			
Disabled	See normal operations					Write leveling not enabled	0	
Enabled (1)	Disabled (1)	N/A	Low	Off	Off	DQS not receiving: not terminated Prime DQ High-Z: not terminated Other DQ High-Z: not terminated	1	2
		20Ω,30Ω 40Ω, 60Ω, or 120Ω	High	On		DQS not receiving: terminated by R_{TT} Prime DQ High-Z: not terminated Other DQ High-Z: not terminated	2	
	Enabled (0)	N/A	Low	Off		DQS receiving: not terminated Prime DQ driving CK state: not terminated Other DQ driving LOW: not terminated	3	3
		40Ω,60Ω, or 120Ω	High	On		DQS receiving: terminated by R_{TT} Prime DQ driving CK state: not terminated Other DQ driving LOW: not terminated	4	

Notes :
1. Expected usage if used during write leveling: Case 1 may be used when DRAM are on a dual-rank module and on the rank not being leveled or on any rank of a module not being leveled on a multislot system. Case 2 may be used when DRAM are on any rank of a module not being leveled on a multislot system. Case 3 is generally not used. Case 4 is generally used when DRAM are on the rank that is being leveled.
2. Since the DRAM DQS is not being driven (MR1[12] = 1), DQS ignores the input strobe, and all RTT,nom values are allowed. This simulates a normal standby state to DQS.
3. Since the DRAM DQS is being driven (MR1[12] = 0), DQS captures the input strobe, and only some RTT,nom values are allowed. This simulates a normal write state to DQS.

Write Leveling Mode Exit Procedure

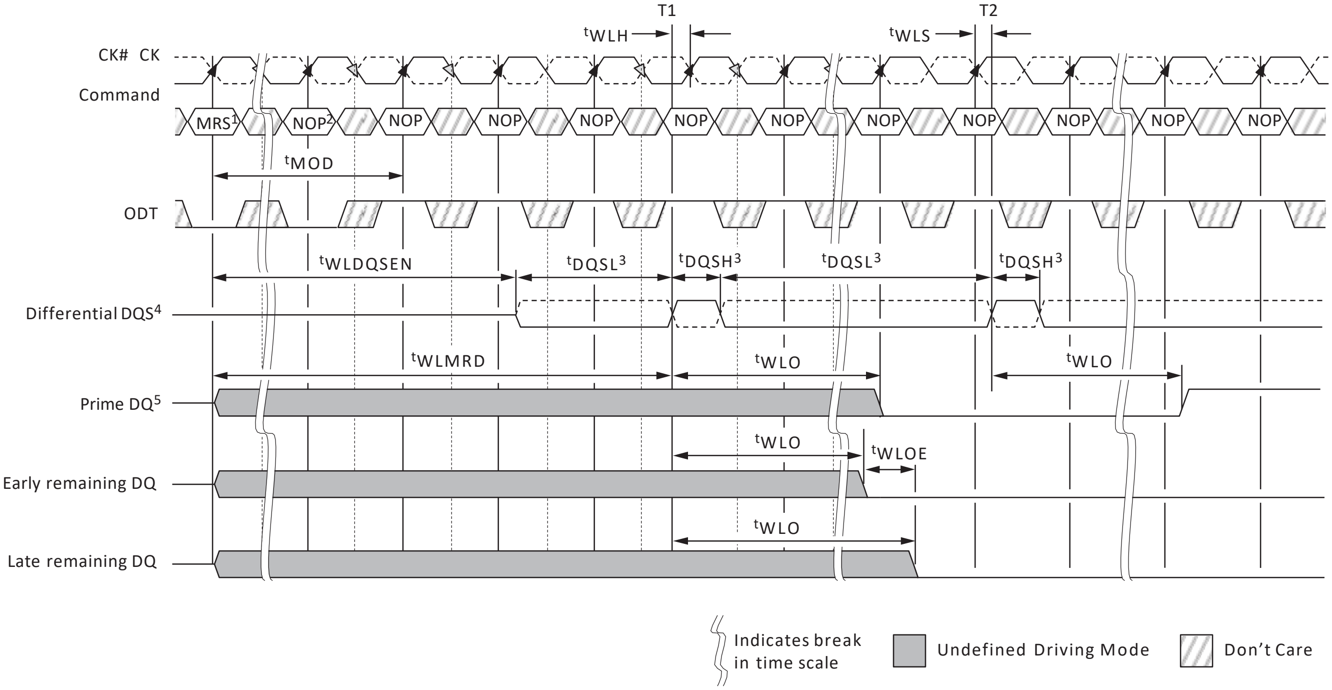
A memory controller initiates the DRAM write leveling mode by setting MR1[7] to 1, assuming the other programmable features (MR0, MR1, MR2, and MR3) are first set and the DLL is fully reset and locked. The DQ balls enter the write leveling mode going from a High-Z state to an undefined driving state, so the DQ bus should not be driven. During write leveling mode, only the NOP or DES commands are allowed. The memory controller should attempt to level only one rank at a time; thus, the outputs of other ranks should be disabled by setting MR1[12] to 1 in the other ranks. The memory controller may assert ODT after a ^{t}MOD delay, as the DRAM will be ready to process the ODT transition. ODT should be turned on prior to DQS being driven LOW by at least ODTLon delay (WL - 2 ^{t}CK), provided it does not violate the aforementioned ^{t}MOD delay requirement.

The memory controller may drive DQS LOW and DQS# HIGH after ^{t}WLDQSEN has been satisfied. The controller may begin to toggle DQS after ^{t}WLMRD (one DQS toggle is DQS transitioning from a LOW state to a HIGH state with DQS# transitioning from a HIGH state to a LOW state, then both transition back to their original states). At a mini- mum, ODTLon and ^{t}AON must be satisfied at least one clock prior to DQS toggling.

After ^{t}WLMRD and a DQS LOW preamble (^{t}WPRE) have been satisfied, the memory controller may provide either a single DQS toggle or multiple DQS toggles to sample CK for a given DQS-to-CK skew. Each DQS toggle must not violate ^{t}DQSL (MIN) and ^{t}DQSH (MIN) specifications. ^{t}DQSL (MAX) and ^{t}DQSH (MAX) specifications are not applicable during write leveling mode. The DQS must be able to distinguish the CK's rising edge within ^{t}WLS and ^{t}WLH. The prime DQ will output the CK's status asynchronously from the associated DQS rising edge CK capture within ^{t}WLO. The remaining DQ that always drive LOW when DQS is toggling must be LOW within ^{t}WLOE after the first ^{t}WLO is satisfied (the prime DQ going LOW). As previously noted, DQS is an input and not an output during this process. Figure 35 depicts the basic timing parameters for the overall write leveling procedure.

The memory controller will most likely sample each applicable prime DQ state and determine whether to increment or decrement its DQS delay setting. After the memory controller performs enough DQS toggles to detect the CK's 0-to-1 transition, the memory controller should lock the DQS delay setting for that DRAM. After locking the DQS setting is locked, leveling for the rank will have been achieved, and the write leveling mode for the rank should be disabled or reprogrammed (if write leveling of another rank follows).

Figure 35 : Write Leveling Sequence



Note :

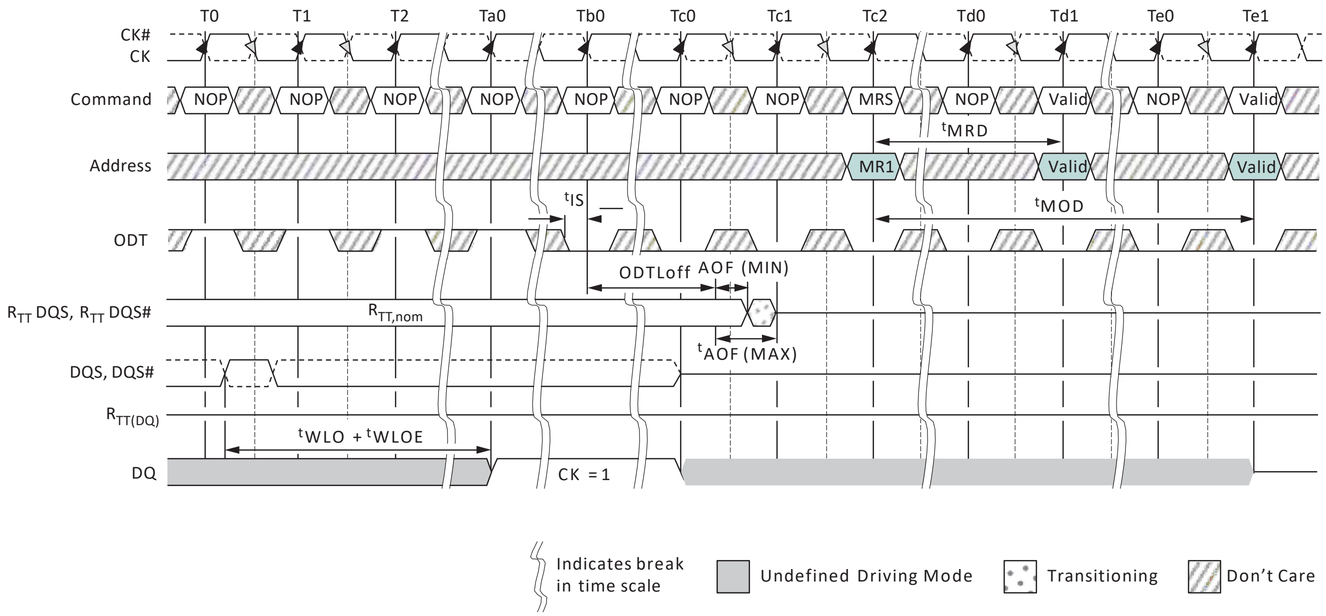
1. MRS: Load MR1 to enter write leveling mode.
2. NOP: NOP or DES.
3. DQS, DQS# needs to fulfill minimum pulse width requirements ^{t}DQSH (MIN) and ^{t}DQSL (MIN) as defined for regular writes. The maximum pulse width is system-dependent.
4. Differential DQS is the differential data strobe (DQS, DQS#). Timing reference points are the zero crossings. The solid line represents DQS; the dotted line represents DQS#.
5. DRAM drives leveling feedback on a prime DQ (DQ0 for x4 and x8). The remaining DQ are driven LOW and remain in this state throughout the leveling procedure.

Write Leveling Mode Exit Procedure

After the DRAM are leveled, they must exit from write leveling mode before the normal mode can be used. Figure 36 depicts a general procedure for exiting write leveling mode. After the last rising DQS (capturing a 1 at T0), the memory controller should stop driving the DQS signals after tWLO (MAX) delay plus enough delay to enable the memory controller to capture the applicable prime DQ state (at ~Tb0). The DQ balls become undefined when DQS no longer remains LOW, and they remain undefined until tMOD after the MRS command (at Te1).

The ODT input should be de-asserted LOW such that ODTLoff (MIN) expires after the DQS is no longer driving LOW. When ODT LOW satisfies tIS, ODT must be kept LOW (at ~Tb0) until the DRAM is ready for either another rank to be leveled or until the normal mode can be used. After DQS termination is switched off, write level mode should be disabled via the MRS command (at Tc2). After tMOD is satisfied (at Te1), any valid command may be registered by the DRAM. Some MRS commands may be issued after tMRD (at Td1).

Figure 36 : Write Leveling Exit Procedure



Note : 1. The DQ result, = 1, between Ta0 and Tc0, is a result of the DQS, DQS# signals capturing CK HIGH just after the T0 state.

Initialization

The following sequence is required for power-up and initialization, as shown in Figure 37.

1. Apply power. RESET# is recommended to be below 0.2 × VDDQ during power ramp to ensure the outputs remain disabled (High-Z) and ODT off (RTT is also High-Z).All other inputs, including ODT, may be undefined.

During power-up, either of the following conditions may exist and must be met :

- Condition A:
  - VDD and VDDQ are driven from a single-power converter output and are ramped with a maximum delta voltage between them of ΔV ≤ 300mV. Slope reversal of any power supply signal is allowed. The voltage levels on all balls other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side, and must be greater than or equal to VSSQ and VSS on the other side.
  - Both VDD and VDDQ power supplies ramp to VDD,min and VDDQ,min within tVDDPR = 200ms.
  - VREFDQ tracks VDD × 0.5, VREFCA tracks VDD × 0.5.
  - VTT is limited to 0.95V when the power ramp is complete and is not applied directly to the device; however, tVTD should be greater than or equal to 0 to avoid device latchup.

- Condition B :
  - VDD may be applied before or at the same time as VDDQ.
  - VDDQ may be applied before or at the same time as VTT, VREFDQ, and VREFCA.
  - No slope reversals are allowed in the power supply ramp for this condition.

2. Until stable power, maintain RESET# LOW to ensure the outputs remain disabled (High-Z). After the power is stable, RESET# must be LOW for at least 200µs to begin the initialization process. ODT will remain in the High-Z state while RESET# is LOW and until CKE is registered HIGH.

3. CKE must be LOW 10ns prior to RESET# transitioning HIGH.

4. After RESET# transitions HIGH, wait 500µs (minus one clock) with CKE LOW.

5. After the CKE LOW time, CKE may be brought HIGH (synchronously) and only NOP or DES commands may be issued. The clock must be present and valid for at least 10ns (and a minimum of five clocks) and ODT must be driven LOW at least tIS prior to CKE being registered HIGH. When CKE is registered HIGH, it must be continuously registered HIGH until the full initialization process is complete.

6. After CKE is registered HIGH and after tXPR has been satisfied, MRS commands may be issued. Issue an MRS (LOAD MODE) command to MR2 with the applicable settings (provide LOW to BA2 and BA0 and HIGH to BA1).

7. Issue an MRS command to MR3 with the applicable settings.

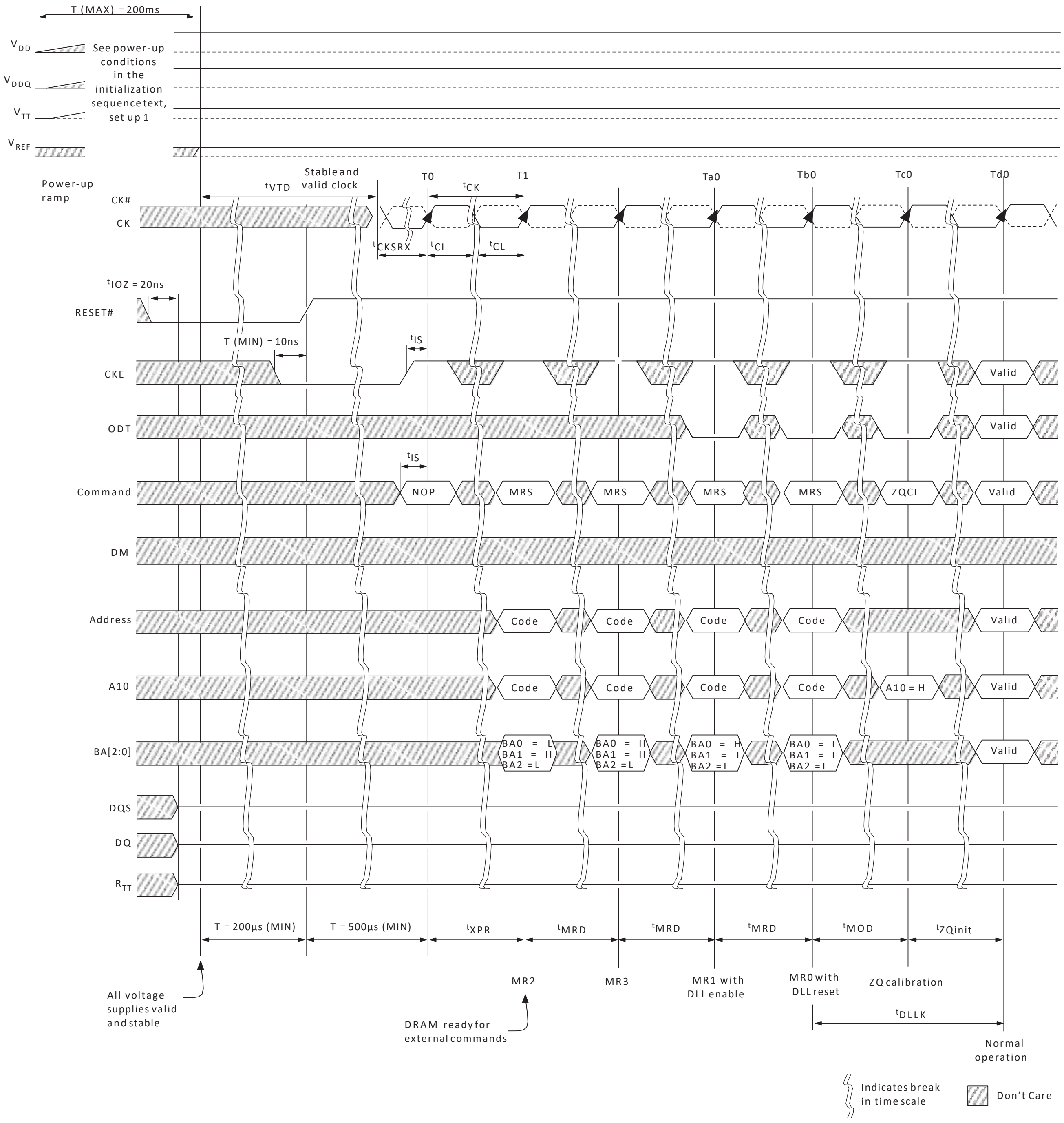
8. Issue an MRS command to MR1 with the applicable settings, including enabling the DLL and configuring ODT.

9. Issue an MRS command to MR0 with the applicable settings, including a DLL RESET command. tDLLK (512) cycles of clock input are required to lock the DLL.

10. Issue a ZQCL command to calibrate RTT and RON values for the process voltage temperature (PVT). Prior to normal operation, tZQinit must be satisfied.

11. When tDLLK and tZQinit have been satisfied, the DDR3 SDRAM will be ready for normal operation.

Figure 37 : Initialization Sequence



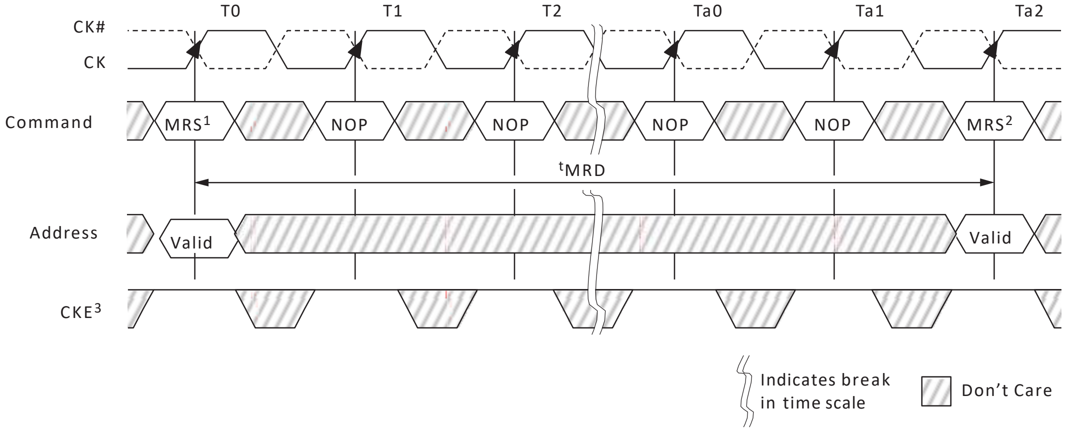
Mode Registers

Mode registers (MR0–MR3) are used to define various modes of programmable operations of the DDR3 SDRAM. A mode register is programmed via the mode register set (MRS) command during initialization, and it retains the stored information (except for MR0[8], which is self-clearing) until it is reprogrammed, RESET# goes LOW, the device loses power.

Contents of a mode register can be altered by re-executing the MRS command. Even if the user wants to modify only a subset of the mode register's variables, all variables must be programmed when the MRS command is issued. Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

The MRS command can only be issued (or re-issued) when all banks are idle and in the precharged state (tRP is satisfied and no data bursts are in progress). After an MRS command has been issued, two parameters must be satisfied: tMRD and tMOD. The controller must wait tMRD before initiating any subsequent MRS commands.

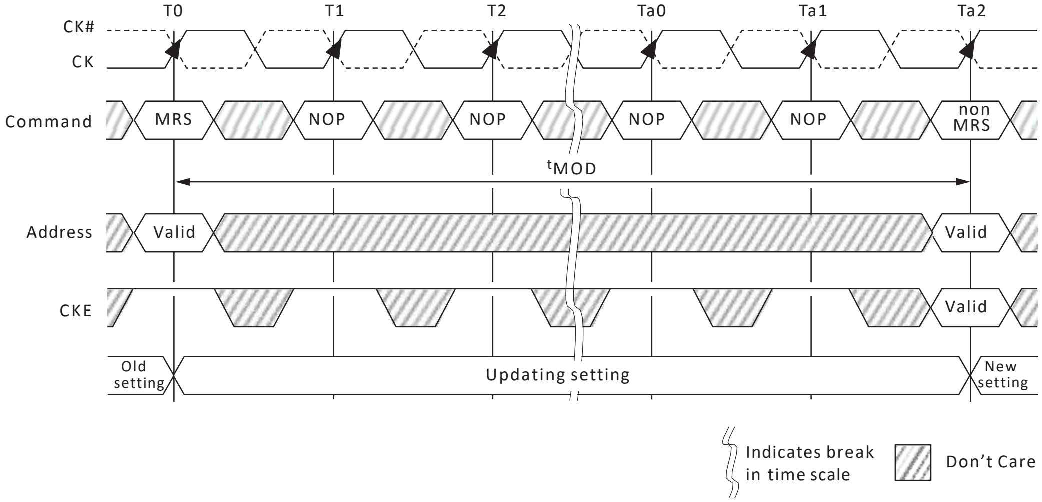
Figure 38 : MRS to MRS Command Timing (tMRD)



Notes : 1. Prior to issuing the MRS command, all banks must be idle and precharged, tRP (MIN) must be satisfied, and no data bursts can be in progress.
2. tMRD specifies the MRS to MRS command minimum cycle time.
3. CKE must be registered HIGH from the MRS command until tMRSPDEN (MIN) (see Power-Down Mode).
4. For a CAS latency change, tXPDLL timing must be met before any non-MRS command.

The controller must also wait tMOD before initiating any non-MRS commands (excluding NOP and DES). The DRAM requires tMOD in order to update the requested features, with the exception of DLL RESET, which requires additional time. Until tMOD has been satisfied, the updated features are to be assumed unavailable.

Figure 39 : MRS to nonMRS Command Timing (tMOD)



Notes :
1. Prior to issuing the MRS command, all banks must be idle (they must be precharged, tRP must be satisfied, and no data bursts can be in progress).
2. Prior to Ta2 when tMOD (MIN) is being satisfied, no commands (except NOP/DES) may be issued.
3. If RTT was previously enabled, ODT must be registered LOW at T0 so that ODTL is satisfied prior to Ta1. ODT must also be registered LOW at each rising CK edge from T0 until tMODmin is satisfied at Ta2.
4. CKE must be registered HIGH from the MRS command until tMRSPDEN (MIN), at which time power-down may occur (see Power-Down Mode).

Mode Register 0 (MR0)

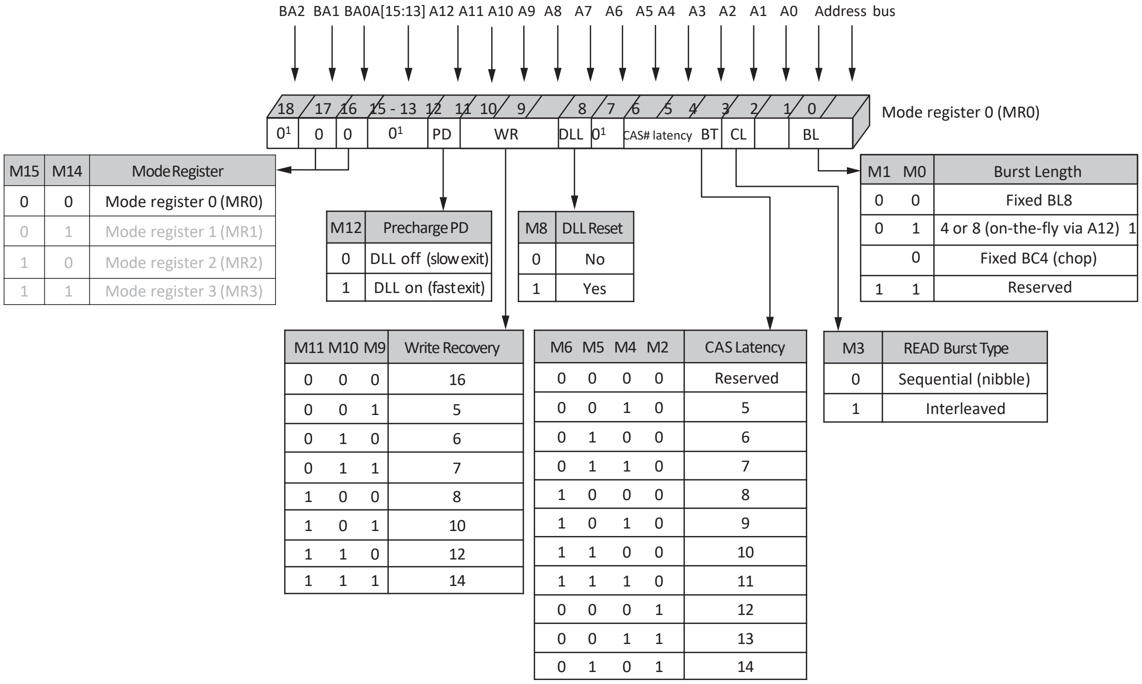
The base register, MR0, is used to define various DDR3 SDRAM modes of operation. These definitions include the selection of a burst length, burst type, CAS latency, operating mode, DLL RESET, write recovery, and precharge power-down mode, as shown in Figure 40.

Burst Length

Burst length is defined by MR0[1: 0]. Read and write accesses to the DDR3 SDRAM are burst-oriented, with the burst length being programmable to 4 (chop mode), 8 (fixed), or selectable using A12 during a READ/ WRITE command (on-the-fly). The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. When MR0[1:0] is set to 01 during a READ/WRITE command, if A12 = 0, then BC4 (chop) mode is selected. If A12 = 1, then BL8 mode is selected. Specific timing diagrams, and turnaround between READ/WRITE, are shown in the READ/WRITE sections of this document.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A[*i*:2] when the burst length is set to 4 and by A[*i*:3] when the burst length is set to 8 (where A*i* is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Figure 40 : Mode Register 0 (MR0) Definitions



M15	M14	Mode Register
0	0	Mode register 0 (MR0)
0	1	Mode register 1 (MR1)
1	0	Mode register 2 (MR2)
1	1	Mode register 3 (MR3)

M12	Precharge PD
0	DLL off (slow exit)
1	DLL on (fast exit)

M8	DLL Reset
0	No
1	Yes

M1	M0	Burst Length
0	0	Fixed BL8
0	1	4 or 8 (on-the-fly via A12) 1
	0	Fixed BC4 (chop)
1	1	Reserved

M11	M10	M9	Write Recovery
0	0	0	16
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

M6	M5	M4	M2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13
0	1	0	1	14

M3	READ Burst Type
0	Sequential (nibble)
1	Interleaved

Note : 1. MR0[18, 15:13, 7] are reserved for future use and must be programmed to 0.

Burst Type

Accesses within a given burst may be programmed to either a sequential or an interleaved order. The burst type is selected via MR0[3] (see Figure 40). The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address. DDR3 only supports 4-bit burst chop and 8-bit burst access modes.

Full interleave address ordering is supported for READs, while WRITEs are restricted to nibble (BC4) or word (BL8) boundaries.

Table 70 : Burst Order

Burst Length	READ/ WRITE	Starting Column Address (A[2, 1, 0])	Burst Type = Sequential (Decimal)	Burst Type = Interleaved(Decimal)	Notes
4 chop	READ	0 0 0	0, 1, 2, 3, Z, Z, Z, Z	0, 1, 2, 3, Z, Z, Z, Z	1, 2
		0 0 1	1, 2, 3, 0, Z, Z, Z, Z	1, 0, 3, 2, Z, Z, Z, Z	1, 2
		0 1 0	2, 3, 0, 1, Z, Z, Z, Z	2, 3, 0, 1, Z, Z, Z, Z	1, 2
		0 1 1	3, 0, 1, 2, Z, Z, Z, Z	3, 2, 1, 0, Z, Z, Z, Z	1, 2
		1 0 0	4, 5, 6, 7, Z, Z, Z, Z	4, 5, 6, 7, Z, Z, Z, Z	1, 2
		1 0 1	5, 6, 7, 4, Z, Z, Z, Z	5, 4, 7, 6, Z, Z, Z, Z	1, 2
		1 1 0	6, 7, 4, 5, Z, Z, Z, Z	6, 7, 4, 5, Z, Z, Z, Z	1, 2
		1 1 1	7, 4, 5, 6, Z, Z, Z, Z	7, 6, 5, 4, Z, Z, Z, Z	1, 2
	WRITE	0 V V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	1, 3,4
		1 V V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	1, 3, 4
8	READ	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	1
		0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	1
		0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	1
		0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	1
		1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	1
		1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	1
		1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	1
		1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	1
	WRITE	V V V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	1, 3

Notes : 1. Internal READ and WRITE operations start at the same point in time for BC4 as they do for BL8.
2. Z = Data and strobe output drivers are in tri-state.
3. V = A valid logic level (0 or 1), but the respective input buffer ignores level-on input pins.
4. X = “Don’t Care.”

DLL RESET

DLL RESET is defined by MR0[8] (see Figure 40). Programming MR0[8] to 1 activates the DLL RESET function. MR0[8] is self-clearing, meaning it returns to a value of 0 after the DLL RESET function has been initiated. Anytime the DLL RESET function is initiated, CKE must be HIGH and the clock held stable for 512 (tDLLK) clock cycles before a READ command can be issued. This is to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in invalid output timing specifications, such as tDQSCK timings.

Write Recovery

WRITE recovery time is defined by MR0[11:9] (see Figure 40). Write recovery values of 5, 6, 7, 8, 10, or 12 may be used by programming MR0[11:9]. The user is required to program the correct value of write recovery and is calculated by dividing tWR (ns) by tCK (ns) and rounding up a noninteger value to the next integer: WR (cycles) = roundup (tWR [ns]/tCK [ns]).

Precharge Power-Down (Precharge PD)

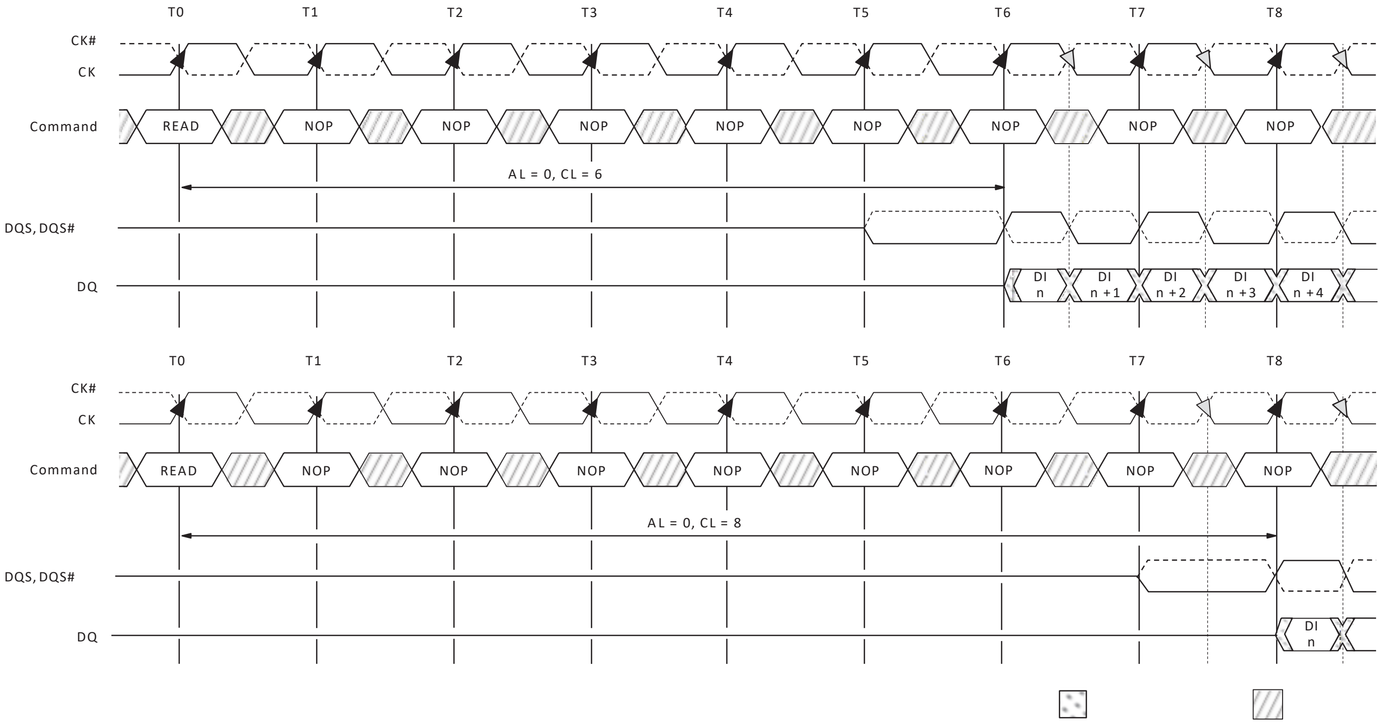
The precharge PD bit applies only when precharge power-down mode is being used. When MR0[12] is set to 0, the DLL is off during precharge power-down providing a lower standby current mode; however, tXPDLL must be satisfied when exiting. When MR0[12] is set to 1, the DLL continues to run during precharge power-down mode to enable a faster exit of precharge power-down mode; however, tXP must be satisfied when exiting (see Power-Down Mode).

CAS Latency (CL)

The CL is defined by MR0[6:4], as shown in Figure 40. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. The CL can be set to 5, 6, 7, 8, 9, or 10. DDR3 SDRAM do not support half-clock latencies.

Examples of CL = 6 and CL = 8 are shown below. If an internal READ command is registered at clock edge *n*, and the CAS latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. on page through Table 46 indicate the CLs supported at various operating frequencies.

Figure 41 : READ Latency



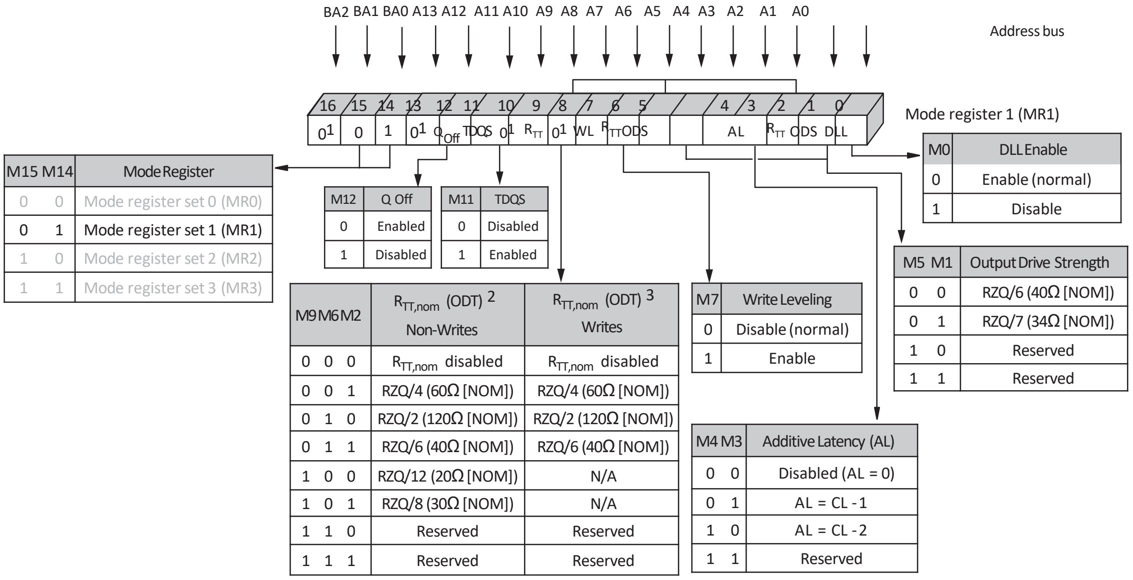
Notes: 1. For illustration purposes, only CL = 6 and CL = 8 are shown. Other CL values are possible.
2. Shown with nominal tDQSCK and nominal tDSDQ.

Mode Register 1 (MR1)

The mode register 1 (MR1) controls additional functions and features not available in the other mode registers: Q OFF (OUTPUT DISABLE), TDQS (for the x8 configuration only), DLL ENABLE/DLL DISABLE, RTT,nom value (ODT), WRITE LEVELING, POSTED CAS ADDITIVE latency, and OUTPUT DRIVE STRENGTH. These functions are controlled via the bits shown in Figure 42. The MR1 register is programmed via the MRS command and retains the stored information until it is reprogrammed, until RESET# goes LOW, or until the device loses power. Reprogramming the MR1 register will not alter the contents of the memory array, provided it is performed correctly.

The MR1 register must be loaded when all banks are idle and no bursts are in progress. The controller must satisfy the specified timing parameters tMRD and tMOD before initiating a subsequent operation.

Figure 42 : Mode Register 1 (MR1) Definition



M15 M14	Mode Register
0 0	Mode register set 0 (MR0)
0 1	Mode register set 1 (MR1)
1 0	Mode register set 2 (MR2)
1 1	Mode register set 3 (MR3)

M12	Q Off
0	Enabled
1	Disabled

M11	TDQS
0	Disabled
1	Enabled

M0	DLL Enable
0	Enable (normal)
1	Disable

M5 M1	Output Drive Strength
0 0	RZQ/6 (40Ω [NOM])
0 1	RZQ/7 (34Ω [NOM])
1 0	Reserved
1 1	Reserved

M9 M6 M2	$R_{TT,nom}$ (ODT) [2] Non-Writes	$R_{TT,nom}$ (ODT) [3] Writes
0 0 0	$R_{TT,nom}$ disabled	$R_{TT,nom}$ disabled
0 0 1	RZQ/4 (60Ω [NOM])	RZQ/4 (60Ω [NOM])
0 1 0	RZQ/2 (120Ω [NOM])	RZQ/2 (120Ω [NOM])
0 1 1	RZQ/6 (40Ω [NOM])	RZQ/6 (40Ω [NOM])
1 0 0	RZQ/12 (20Ω [NOM])	N/A
1 0 1	RZQ/8 (30Ω [NOM])	N/A
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

M7	Write Leveling
0	Disable (normal)
1	Enable

M4 M3	Additive Latency (AL)
0 0	Disabled (AL = 0)
0 1	AL = CL - 1
1 0	AL = CL - 2
1 1	Reserved

Notes: 1. MR1[16, 13, 10, 8] are reserved for future use and must be programmed to 0.
2. During write leveling, if MR1[7] and MR1[12] are 1, then all RTT,nom values are available for use.
3. During write leveling, if MR1[7] is a 1, but MR1[12] is a 0, then only RTT,nom write values are available for use.

DLL Enable/DLL Disable

The DLL may be enabled or disabled by programming MR1[0] during the LOAD MODE command, as shown in Figure 42. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using the appropriate LOAD MODE command.

If the DLL is enabled prior to entering self refresh mode, the DLL is automatically disabled when entering SELF REFRESH operation and is automatically reenabled and reset upon exit of SELF REFRESH operation. If the DLL is disabled prior to entering self refresh mode, the DLL remains disabled even upon exit of SELF REFRESH operation until it is reenabled and reset.

The DRAM is not tested to check—nor does Dosilicon warrant compliance with—normal mode timings or functionality when the DLL is disabled. An attempt has been made to have the DRAM operate in the normal mode where reasonably possible when the DLL has been disabled; however, by industry standard, a few known exceptions are defined:

- ODT is not allowed to be used
- The output data is no longer edge-aligned to the clock
- CL and CWL can only be six clocks

When the DLL is disabled, timing and functionality can vary from the normal operation specifications when the DLL is enabled(see DLL Disable Mode). Disabling the DLL also implies the need to change the clock frequency (see Input Clock Frequency Change).

Output Drive Strength

The DDR3 SDRAM uses a programmable impedance output buffer. The drive strength mode register setting is defined by MR1[5, 1]. RZQ/7 (34Ω [NOM]) is the primary output driver impedance setting for DDR3 SDRAM devices. To calibrate the output driver impedance, an external precision resistor (RZQ) is connected between the ZQ ball and VSSQ. The value of the resistor must be 240Ω ± 1%.

The output impedance is set during initialization. Additional impedance calibration updates do not affect device operation, and all data sheet timings and current specifications are met during an update.

To meet the 34Ω specification, the output drive strength must be set to 34Ω during initialization. To obtain a calibrated output driver impedance after power-up, the DDR3 SDRAM needs a calibration command that is part of the initialization and reset procedure.

OUTPUT ENABLE/DISABLE

The OUTPUT ENABLE function is defined by MR1[12], as shown in Figure 42. When enabled (MR1[12] = 0), all outputs (DQ, DQS, DQS#) function when in the normal mode of operation. When disabled (MR1[12] = 1), all DDR3 SDRAM outputs (DQ and DQS, DQS#) are tri-stated. The output disable feature is intended to be used during IDD characterization of the READ current and during tDQSS margining (write leveling) only.

TDQS Enable

Termination data strobe (TDQS) is a feature of the x8 DDR3 SDRAM configuration that provides termination resistance (RTT) and may be useful in some system configurations. TDQS is not supported in x4 or x16 configurations. When enabled via the mode register (MR1[11]), the RTT that is applied to DQS and DQS# is also applied to TDQS and TDQS#. In contrast to the RDQS function of DDR2 SDRAM, DDR3's TDQS provides the termination resistance RTT only. The OUTPUT DATA STROBE function of RDQS is not provided by TDQS; thus, RON does not apply to TDQS and TDQS#. The TDQS and DM functions share the same ball. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided, and the TDQS# ball is not used. The TDQS function is available in the x8 DDR3 SDRAM configuration only and must be disabled via the mode register for the x4 and x16 configurations.

On-Die Termination

ODT resistance RTT,nom is defined by MR1[9, 6, 2] (see Figure 42). The RTT termination value applies to the DQ, DM, DQS, DQS#, and TDQS, TDQS# balls. DDR3 supports multiple RTT termination values based on RZQ/*n* where *n* can be 2, 4, 6, 8, or 12 and RZQ is 240Ω. Unlike DDR2, DDR3 ODT must be turned off prior to reading data out and must remain off during a READ burst. RTT,nom termination is allowed any time after the DRAM is initialized, calibrated, and not performing read access, or when it is not in self refresh mode. Additionally, write accesses with dynamic ODT enabled (RTT(WR)) temporarily replaces RTT,nom with RTT(WR).

The actual effective termination, RTT(EFF), may be different from the RTT targeted due to nonlinearity of the termination. For RTT(EFF) values and calculations (see On-Die Termination (ODT).

The ODT feature is designed to improve signal integrity of the memory channel by enabling the DDR3 SDRAM controller to independently turn on/off ODT for any or all devices. The ODT input control pin is used to determine when RTT is turned on (ODTL on) and off (ODTL off), assuming ODT has been enabled via MR1[9, 6, 2].

Timings for ODT are detailed in On-Die Termination (ODT).

WRITE LEVELING

The WRITE LEVELING function is enabled by MR1[7], as shown in Figure 42. Write leveling is used (during initialization) to deskew the DQS strobe to clock offset as a result of fly-by topology designs. For better signal integrity, DDR3 SDRAM memory modules adopted fly-by topology for the commands, addresses, control signals, and clocks.

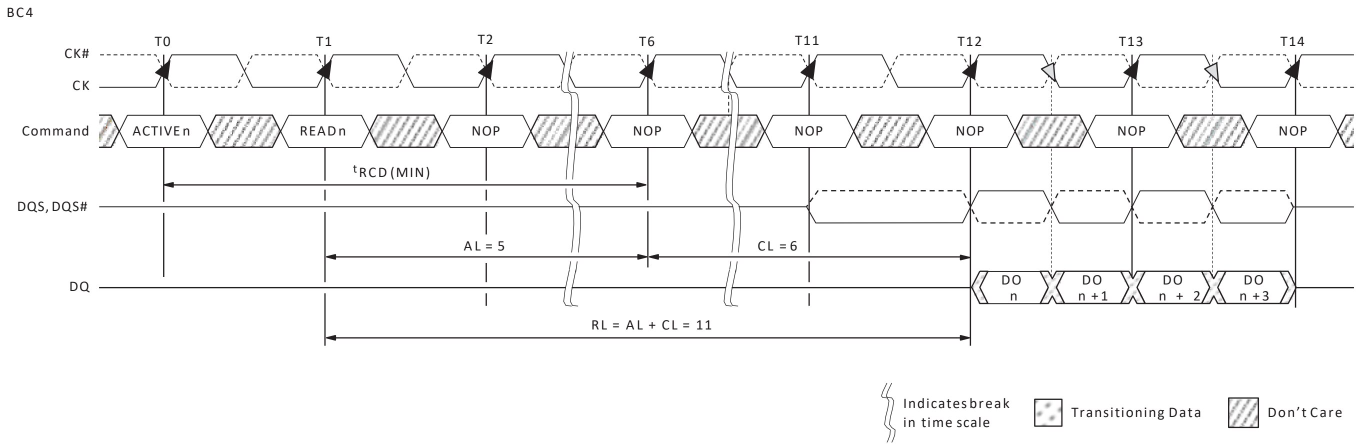
The fly-by topology benefits from a reduced number of stubs and their lengths. However, fly-by topology induces flight time skews between the clock and DQS strobe (and DQ) at each DRAM on the DIMM. Controllers will have a difficult time maintaining tDQSS, tDSS, and tDSH specifications without supporting write leveling in systems which use fly-by topology-based modules. Write leveling timing and detailed operation information is provided in Write Leveling

POSTED CAS ADDITIVE Latency

POSTED CAS ADDITIVE latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. MR1[4, 3] define the value of AL, as shown in Figure 43. MR1[4, 3] enable the user to program the DDR3 SDRAM with AL = 0, CL - 1, or CL - 2..

With this feature, the DDR3 SDRAM enables a READ or WRITE command to be issued after the ACTIVATE command for that bank prior to tRCD (MIN). The only restriction is ACTIVATE to READ or WRITE + AL ≥ tRCD (MIN) must be satisfied. Assuming tRCD (MIN) = CL, a typical application using this feature sets AL=CL-1tCK= tRCD (MIN)–1 tCK. The READ or WRITE command is held for the time of the AL before it is released internally to the DDR3 SDRAM device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL), RL = AL + CL. WRITE latency (WL) is the sum of CAS WRITE latency and AL, WL = AL + CWL (see Mode Register 2 (MR2). Examples of READ and WRITE latencies are shown in Figure 43 and Figure 45.)

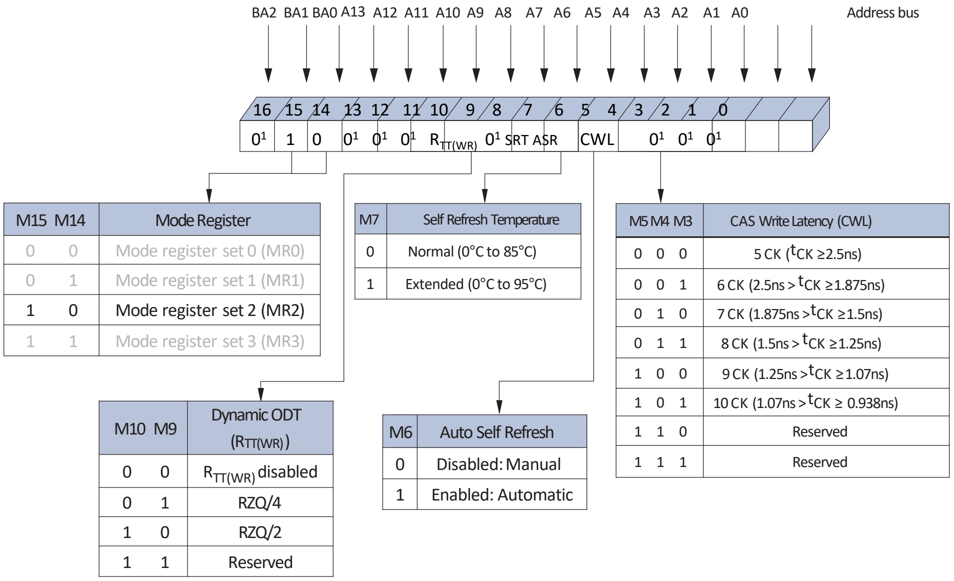
Figure 43 : READ Latency (AL = 5, CL = 6)



Mode Register 2 (MR2)

The mode register 2 (MR2) controls additional functions and features not available in the other mode registers. These additional functions are CAS WRITE latency (CWL), AUTO SELF REFRESH (ASR), SELF REFRESH TEMPERATURE (SRT), and DYNAMIC ODT (RTT(WR)). These functions are controlled via the bits shown in Figure 44. The MR2 is programmed via the MRS command and will retain the stored information until it is programmed again or until the device loses power. Reprogramming the MR2 register will not alter the contents of the memory array, provided it is performed correctly. The MR2 register must be loaded when all banks are idle and no data bursts are in progress, and the controller must wait the specified time tMRD and tMOD before initiating a subsequent operation.

Figure 44 : Mode Register 2 (MR2) Definition



M15 M14	Mode Register
0 0	Mode register set 0 (MR0)
0 1	Mode register set 1 (MR1)
1 0	Mode register set 2 (MR2)
1 1	Mode register set 3 (MR3)

M7	Self Refresh Temperature
0	Normal (0°C to 85°C)
1	Extended (0°C to 95°C)

M5 M4 M3	CAS Write Latency (CWL)
0 0 0	5 CK (tCK ≥2.5ns)
0 0 1	6 CK (2.5ns > tCK ≥1.875ns)
0 1 0	7 CK (1.875ns > tCK ≥1.5ns)
0 1 1	8 CK (1.5ns > tCK ≥1.25ns)
1 0 0	9 CK (1.25ns > tCK ≥1.07ns)
1 0 1	10 CK (1.07ns > tCK ≥ 0.938ns)
1 1 0	Reserved
1 1 1	Reserved

M10 M9	Dynamic ODT ($R_{TT(WR)}$)
0 0	$R_{TT(WR)}$ disabled
0 1	RZQ/4
1 0	RZQ/2
1 1	Reserved

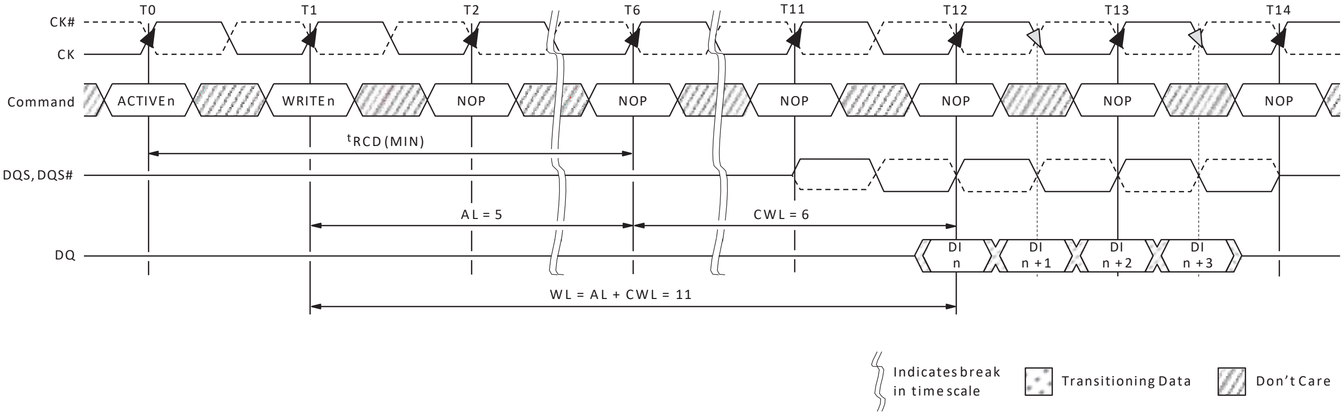
M6	Auto Self Refresh
0	Disabled: Manual
1	Enabled: Automatic

Note: 1. MR2[16, 13:11, 8, and 2:0] are reserved for future use and must all be programmed to 0.

CAS Write Latency (CWL)

CWL is defined by MR2[5:3] and is the delay, in clock cycles, from the releasing of the internal write to the latching of the first data in. CWL must be correctly set to the corresponding operating clock frequency (see Figure 44). The overall WRITE latency (WL) is equal to CWL + AL (Figure 42).

Figure 45 : CAS Write Latency



AUTO SELF REFRESH (ASR)

Mode register MR2[6] is used to disable/enable the ASR function. When ASR is disabled, the self refresh mode's refresh rate is assumed to be at the normal 85°C limit (sometimes referred to as 1x refresh rate). In the disabled mode, ASR requires the user to ensure the DRAM never exceeds a TC of 85°C while in self refresh unless the user enables the SRT feature listed below when the TC is between 85°C and 95°C.

Enabling ASR assumes the DRAM self refresh rate is changed automatically from 1x to 2x when the case temperature exceeds 85°C. This enables the user to operate the DRAM beyond the standard 85°C limit up to the optional extended temperature range of 95°C while in self refresh mode.

The standard self refresh current test specifies test conditions to normal case temperature (85°C) only, meaning if ASR is enabled, the standard self refresh current specifications do not apply (see Extended Temperature Usage.

SELF REFRESH TEMPERATURE (SRT)

Mode register MR2[7] is used to disable/enable the SRT function. When SRT is disabled, the self refresh mode's refresh rate is assumed to be at the normal 85°C limit (sometimes referred to as 1x refresh rate). In the disabled mode, SRT requires the user to ensure the DRAM never exceeds a TC of 85°C while in self refresh mode unless the user enables ASR.

When SRT is enabled, the DRAM self refresh is changed internally from 1x to 2x, regardless of the case temperature. This enables the user to operate the DRAM beyond the standard 85°C limit up to the optional extended temperature range of 95°C while in selfrefresh mode. The standard self refresh current test specifies test conditions to normal case temperature (85°C) only, meaning if SRT is enabled, the standard self refresh current specifications do not apply (see Extended Temperature Usage).

SRT vs. ASR

If the normal case temperature limit of 85°C is not exceeded, then neither SRT nor ASR is required, and both can be disabled throughout operation. However, if the extended temperature option of 95°C is needed, the user is required to provide a 2x refresh rate during (manual) refresh and to enable either the SRT or the ASR to ensure self refresh is performed at the 2x rate.

SRT forces the DRAM to switch the internal self refresh rate from 1x to 2x. Self refresh is performed at the 2x refresh rate regardless of the case temperature.

ASR automatically switches the DRAM's internal self refresh rate from 1x to 2x. However, while in self refresh mode, ASR enables the refresh rate to automatically adjust between 1x to 2x over the supported temperature range. One other disadvantage with ASR is the DRAM cannot always switch from a 1x to a 2x refresh rate at an exact case temperature of 85°C. Although the DRAM will support data integrity when it switches from a 1x to a 2x refresh rate, it may switch at a lower temperature than 85°C.

Since only one mode is necessary, SRT and ASR cannot be enabled at the same time.

DYNAMIC ODT

The dynamic ODT (RTT(WR)) feature is defined by MR2[10, 9]. Dynamic ODT is enabled when a value is selected. This new DDR3 SDRAM feature enables the ODT termination value to change without issuing an MRS command, essentially changing the ODT termination on-the-fly.

With dynamic ODT (RTT(WR)) enabled, the DRAM switches from normal ODT (RTT,nom) to dynamic ODT (RTT(WR)) when beginning a WRITE burst and subsequently switches back to ODT (RTT,nom) at the completion of the WRITE burst. If RTT,nom is disabled, the RTT,nom value will be High-Z. Special timing parameters must be adhered to when dynamic ODT (RTT(WR)) is enabled: ODTLcnw, ODTLcnw4, ODTLcnw8, ODTH4, ODTH8, and tADC.

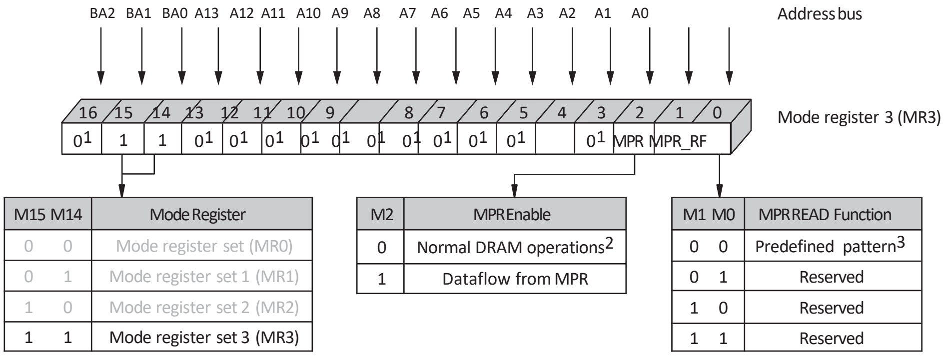
Dynamic ODT is only applicable during WRITE cycles. If ODT (RTT,nom) is disabled, dynamic ODT (RTT(WR)) is still permitted. RTT,nom and RTT(WR) can be used independent of one other. Dynamic ODT is not available during write leveling mode, regardless of the state of ODT (RTT,nom). For details on dynamic ODT operation, refer to On-Die Termination (ODT).

Enabling ASR assumes the DRAM self refresh rate is changed automatically from 1x to 2x when the case temperature exceeds 85°C. This enables the user to operate the DRAM beyond the standard 85°C limit up to the optional extended temperature range of 95°C while in self refresh mode.
The standard self refresh current test specifies test conditions to normal case temperature (85°C) only, meaning if ASR is enabled, the standard self refresh current specifications do not apply (see Extended Temperature Usage.

Mode Register 3 (MR3)

The mode register 3 (MR3) controls additional functions and features not available in the other mode registers. Currently defined is the MULTIPURPOSE REGISTER (MPR). This function is controlled via the bits shown in Figure 46. The MR3 is programmed via the LOAD MODE command and retains the stored information until it is programmed programmed again or until the device loses power. Reprogramming the MR3 register will not alter the contents of the memory array, provided it is performed correctly. The MR3 register must be loaded when all banks are idle and no data bursts are in progress, and the controller must wait the specified time tMRD and tMOD before initiating a subsequent operation.

Figure 46 : Mode Register 3 (MR3) Definition



M15 M14	Mode Register
0 0	Mode register set (MR0)
0 1	Mode register set 1 (MR1)
1 0	Mode register set 2 (MR2)
1 1	Mode register set 3 (MR3)

M2	MPR Enable
0	Normal DRAM operations[2]
1	Dataflow from MPR

M1 M0	MPR READ Function
0 0	Predefined pattern[3]
0 1	Reserved
1 0	Reserved
1 1	Reserved

Notes : 1. MR3[16 and 13:3] are reserved for future use and must all be programmed to 0.
2. When MPR control is set for normal DRAM operation, MR3[1, 0] will be ignored.
3. Intended to be used for READ synchronization

.

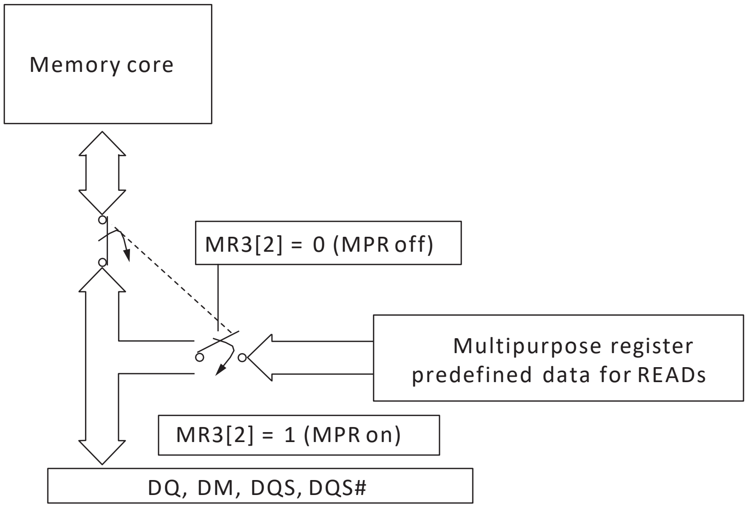
MULTIPURPOSE REGISTER (MPR)

The MULTIPURPOSE REGISTER function is used to output a predefined system timing calibration bit sequence. Bit 2 is the master bit that enables or disables access to the MPR register, and bits 1 and 0 determine which mode the MPR is placed in. The basic concept of the multipurpose register is shown in Figure 47.

If MR3[2] is a 0, then the MPR access is disabled, and the DRAM operates in normal mode. However, if MR3[2] is a 1, then the DRAM no longer outputs normal read data but outputs MPR data as defined by MR3[0, 1]. If MR3[0, 1] is equal to 00, then a predefined read pattern for system calibration is selected.

To enable the MPR, the MRS command is issued to MR3, and MR3[2] = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks are precharged, and tRP is met). When the MPR is enabled, any subsequent READ or RDAP commands are redirected to the multipurpose register. The resulting operation when either a READ or a RDAP command is issued, is defined by MR3[1:0] when the MPR is enabled (see Table 72). When the MPR is enabled, only READ or RDAP commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3[2] = 0). Power-down mode, self refresh, and any other non READ/RDAP commands are not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

Figure 47 : Multipurpose Register (MPR) Block Diagram



Notes :
1. A predefined data pattern can be read out of the MPR with an external READ command.
2. MR3[2] defines whether the data flow comes from the memory core or the MPR. When the data flow is defined, the MPR contents can be read out continuously with a regular READ or RDAP command.

Table 71 : MPR Functional Description of MR3 Bits

MR3[2]	MR3[1:0]	Function
MPR	MPR READ Function	
0	“Don’t Care”	Normal operation, no MPR transaction All subsequent READs come from the DRAM memory array All subsequent WRITEs go to the DRAM memory array
1	A[1:0] (see Table 72)	Enable MPR mode, subsequent READ/RDAP commands defined by bits1 and 2

MPR Functional Description

The MPR JEDEC definition enables either a prime DQ (DQ0 on a x4 and a x8; on a x16, DQ0 = lower byte and DQ8=upper byte) to output the MPR data with the remaining DQs driven LOW, or for all DQs to output the MPR data. The MPR readout supports fixed READ burst and READ burst chop (MRS and OTF via A12/BC#) with regular READ latencies and AC timings applicable, provided the DLL is locked as required.

MPR addressing for a valid MPR read is as follows :

- A[1:0] must be set to 00 as the burst order is fixed per nibble
- A2 selects the burst order:
  - BL8, A2 is set to 0, and the burst order is fixed to 0, 1, 2, 3, 4, 5, 6, 7
- For burst chop 4 cases, the burst order is switched on the nibble base along with the following:
  - A2 = 0; burst order = 0, 1, 2, 3
  - A2 = 1; burst order = 4, 5, 6, 7
- Burst order bit 0 (the first bit) is assigned to LSB, and burst order bit 7 (the last bit) is assigned to MSB
- A[9:3] are a “Don’t Care”
- A10 is a “Don’t Care”
- A11 is a “Don’t Care”
- A12: Selects burst chop mode on-the-fly, if enabled within MR0
- A13 is a “Don’t Care”
- BA[2:0] are a “Don’t Care”

MPR Register Address Definitions and Bursting Order

The MPR currently supports a single data format. This data format is a predefined read pattern for system calibration. The predefined pattern is always a repeating 0–1 bit pattern.

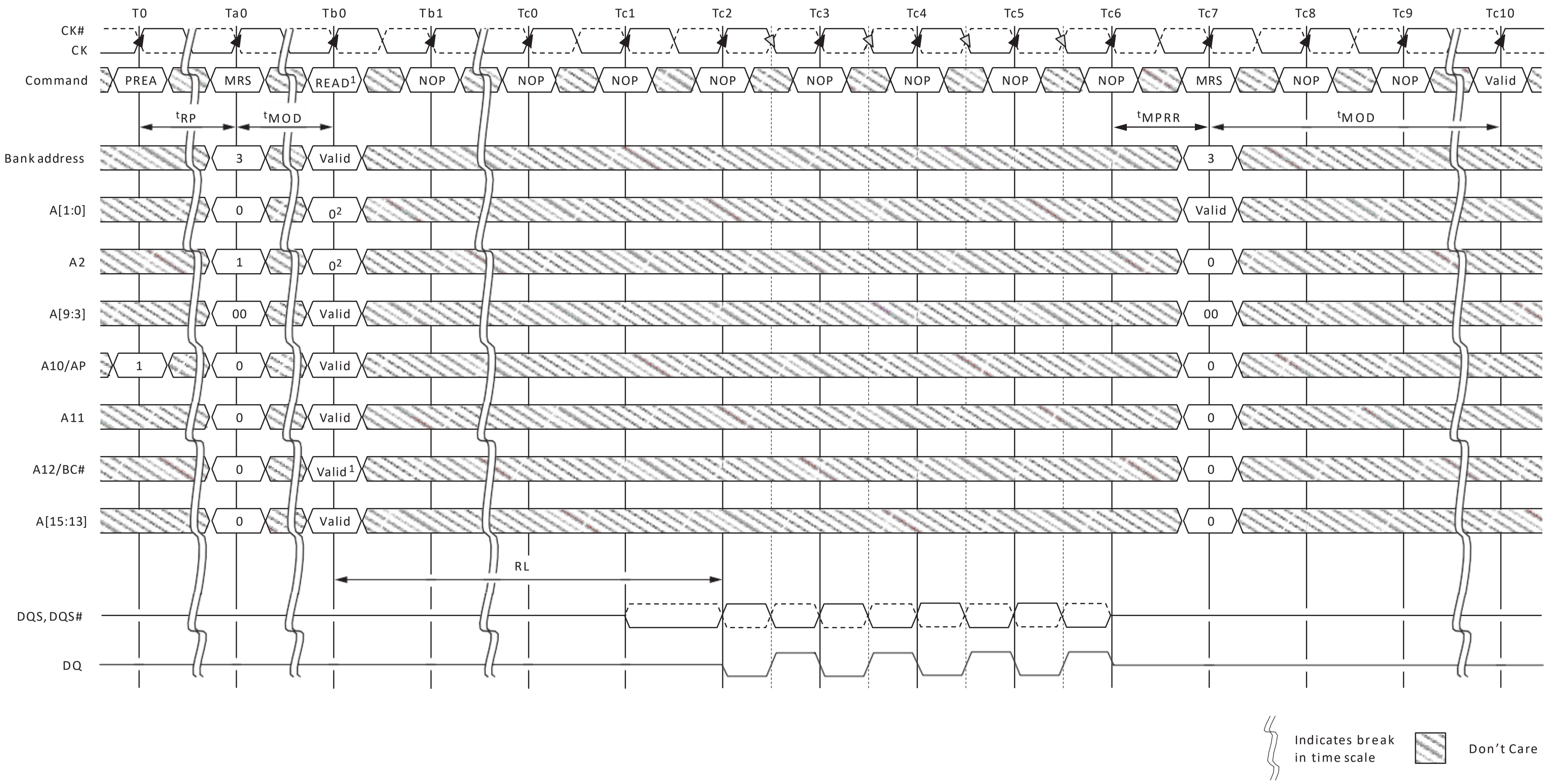
Examples of the different types of predefined READ pattern bursts are shown in the following figures.

Table 72 : MPR Readouts and Burst Order Bit Mapping

MR3[2]	MR3[1:0]	Function	Burst Length	Read A[2:0]	Burst Order and Data Pattern
1	00	READ predefined pattern for system calibration	BL8	000	Burst order: 0, 1, 2, 3, 4, 5, 6, 7 Predefined pattern: 0, 1, 0, 1, 0, 1, 0, 1
			BC4	000	Burst order: 0, 1, 2, 3 Predefined pattern: 0, 1, 0, 1
			BC4	100	Burst order: 4, 5, 6, 7 Predefined pattern: 0, 1, 0, 1
1	01	RFU	N/A	N/A	N/A
			N/A	N/A	N/A
			N/A	N/A	N/A
1	10	RFU	N/A	N/A	N/A
			N/A	N/A	N/A
			N/A	N/A	N/A
1	11	RFU	N/A	N/A	N/A
			N/A	N/A	N/A
			N/A	N/A	N/A

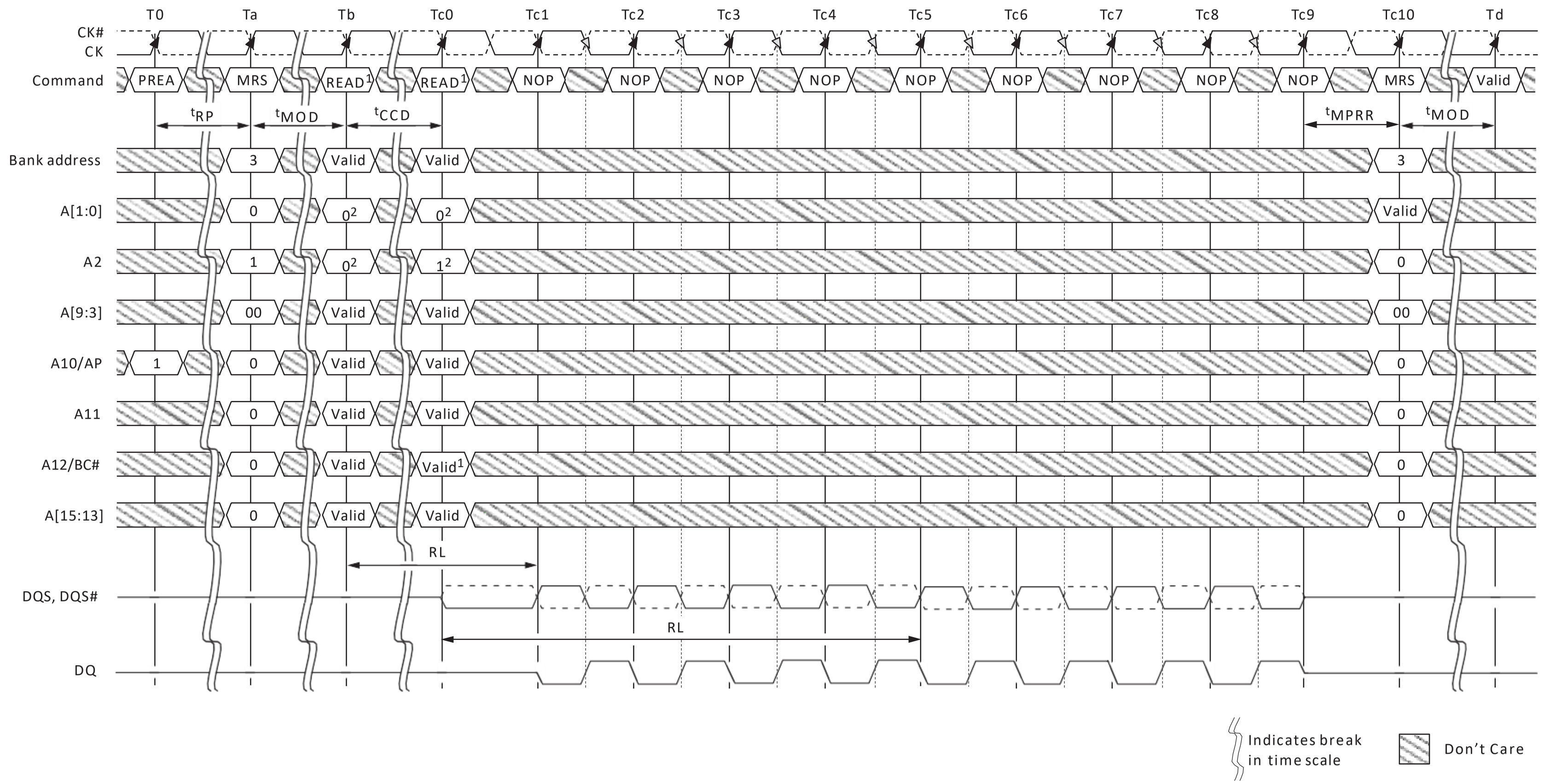
Note: 1. Burst order bit 0 is assigned to LSB, and burst order bit 7 is assigned to MSB of the selected MPR agent.

Figure 48 : MPR System Read Calibration with BL8: Fixed Burst Order Single Readout



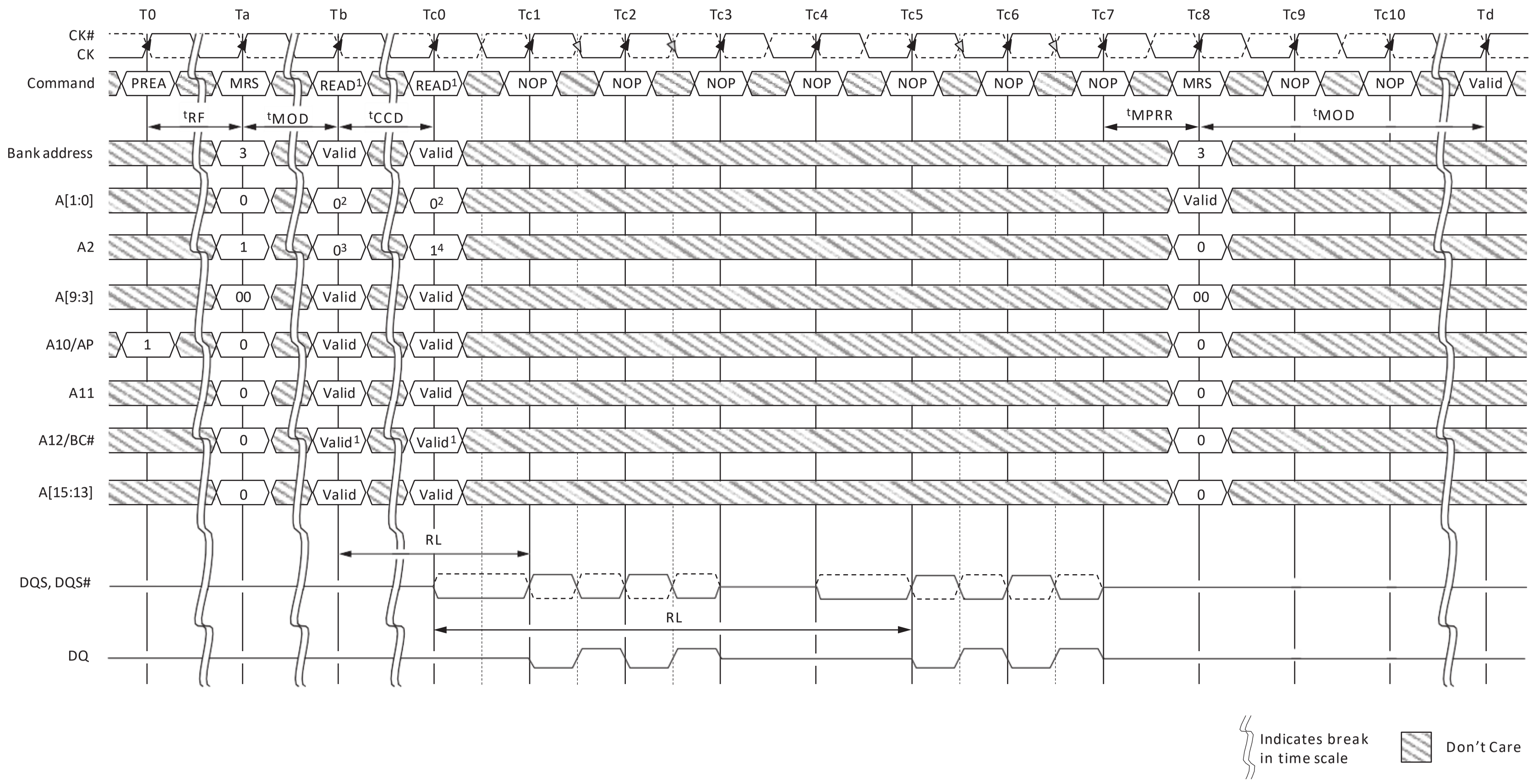
Notes: 1. READ with BL8 either by MRS or OTF.
2. Memory controller must drive 0 on A[2:0].

Figure 49 : MPR System Read Calibration with BL8: Fixed Burst Order, Back-to-Back Readout



Notes: 1. READ with BL8 either by MRS or OTF.
2. Memory controller must drive 0 on A[2:0].

Figure 50 : MPR System Read Calibration with BC4: Lower Nibble, Then Upper Nibble



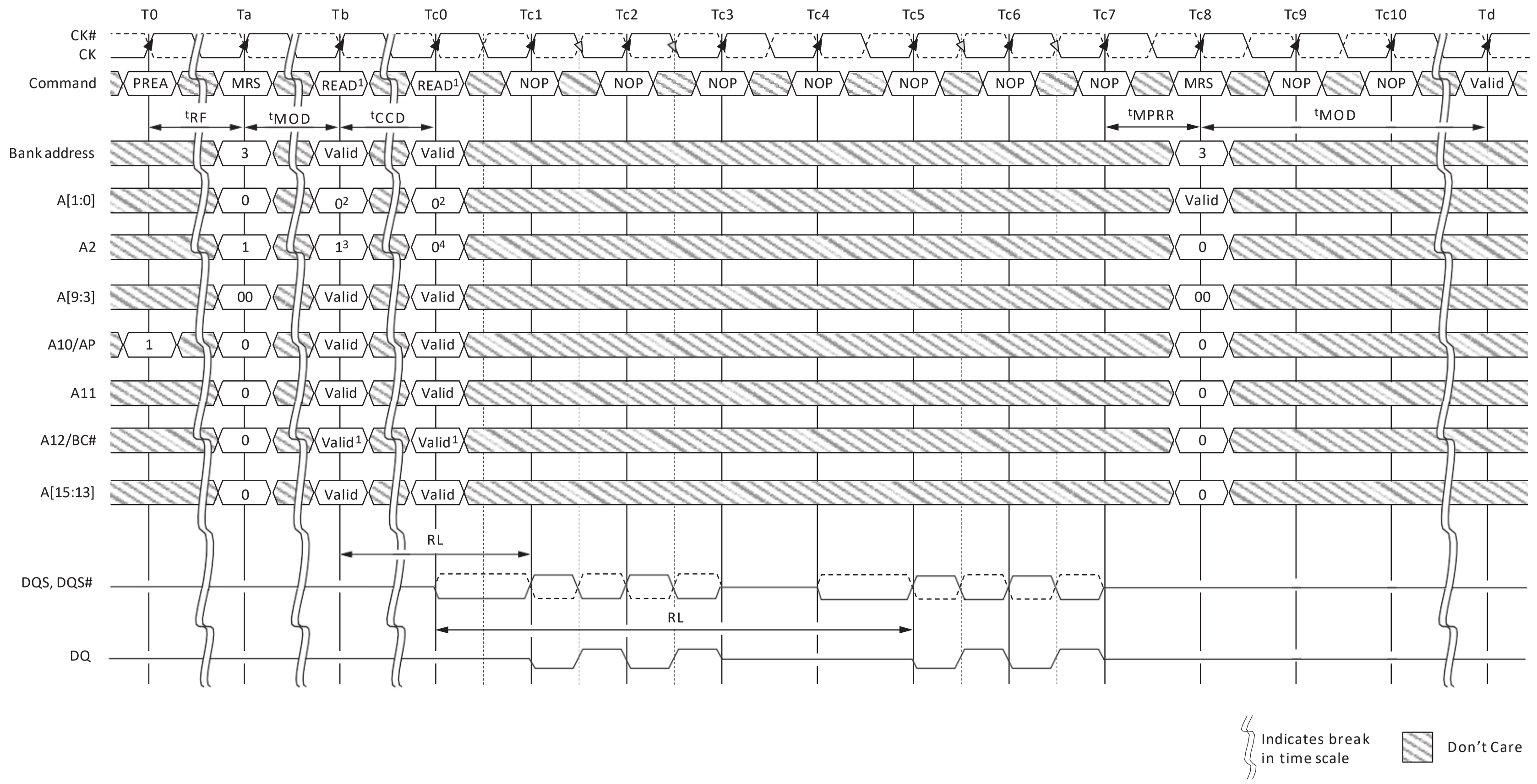
Notes: 1. READ with BC4 either by MRS or OTF.

2. Memory controller must drive 0 on A[1:0].

3. A2 = 0 selects lower 4 nibble bits 0 . . . 3.

4. A2 = 1 selects upper 4 nibble bits 4 . . . 7.

Figure 51 : MPR System Read Calibration with BC4: Upper Nibble, Then Lower Nibble



Notes: 1. READ with BC4 either by MRS or OTF.
2. Memory controller must drive 0 on A[1:0].
3. A2 = 1 selects upper 4 nibble bits 4 . . . 7.
4. A2 = 0 selects lower 4 nibble bits 0 . . . 3.

MPR Read Predefined Pattern

The predetermined read calibration pattern is a fixed pattern of 0, 1, 0, 1, 0, 1, 0, 1. The following is an example of using the read out predetermined read calibration pattern. The example is to perform multiple reads from the multipurpose register to do system level read timing calibration based on the predetermined and standardized pattern.

The following protocol outlines the steps used to perform the read calibration :

1. Precharge all banks
2. After tRP is satisfied, set MRS, MR3[2] = 1 and MR3[1:0] = 00. This redirects all subsequent reads and loads the predefined pattern into the MPR. As soon as tMRD and tMOD are satisfied, the MPR is available
3. Data WRITE operations are not allowed until the MPR returns to the normal DRAM state
4. Issue a read with burst order information (all other address pins are “Don’t Care”):
   - A[1:0] = 00 (data burst order is fixed starting at nibble)
   - A2 = 0 (for BL8, burst order is fixed as 0, 1, 2, 3, 4, 5, 6, 7)
   - A12 = 1 (use BL8)
5. After RL = AL + CL, the DRAM bursts out the predefined read calibration pattern (0, 1, 0, 1, 0, 1, 0, 1)
6. The memory controller repeats the calibration reads until read data capture at memory controller is optimized
7. After the last MPR READ burst and after tMPRR has been satisfied, issue MRS, MR3[2] = 0, and MR3[1:0] = “Don’t Care” to the normal DRAM state. All subsequent read and write accesses will be regular reads and writes from/to the DRAM array
8. When tMRD and tMOD are satisfied from the last MRS, the regular DRAM commands (such as activate a memory bank for regular read or write access) are permitted

MODE REGISTER SET (MRS) Command

The mode registers are loaded via inputs BA[2:0], A[13:0]. BA[2:0] determine which mode register is programmed:

- BA2 = 0, BA1 = 0, BA0 = 0 for MR0
- BA2 = 0, BA1 = 0, BA0 = 1 for MR1
- BA2 = 0, BA1 = 1, BA0 = 0 for MR2
- BA2 = 0, BA1 = 1, BA0 = 1 for MR3

The MRS command can only be issued (or re-issued) when all banks are idle and in the precharged state (tRP is satisfied and no data bursts are in progress). The controller must wait the specified time tMRD before initiating a subsequent operation such as an ACTIVATE command (see Figure 38). There is also a restriction after issuing an MRS command with regard to when the updated functions become available. This parameter is specified by tMOD. Both tMRD and tMOD parameters are shown in Figure 38 and Figure 39. Violating either of these requirements will result in unspecified operation.

ZQ CALIBRATION Operation

The ZQ CALIBRATION command is used to calibrate the DRAM output drivers (RON) and ODT values (RTT) over process, voltage, and temperature, provided a dedicated 240Ω (±1%) external resistor is connected from the DRAM's ZQ ball to VSSQ.

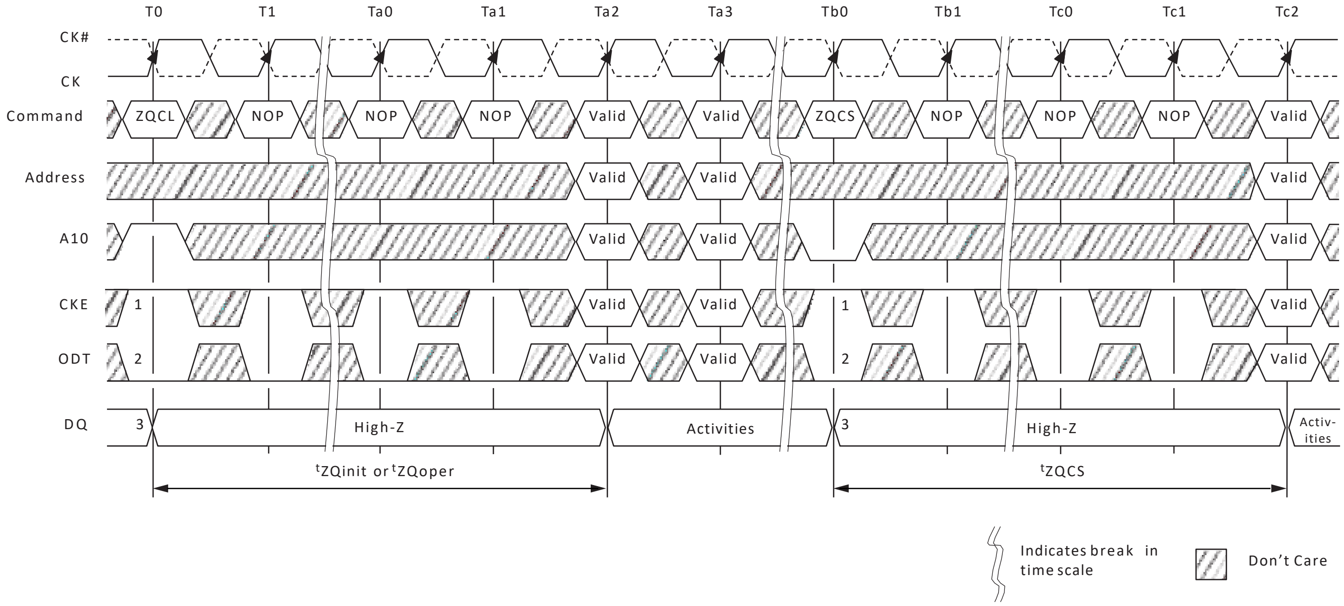
DDR3 SDRAM require a longer time to calibrate RON and ODT at power-up initialization and self refresh exit, and a relatively shorter time to perform periodic calibrations. DDR3 SDRAM defines two ZQ CALIBRATION commands : ZQCL and ZQCS. An example of ZQ calibration timing is shown below.

All banks must be precharged and tRP must be met before ZQCL or ZQCS commands can be issued to the DRAM. No other activities (other than issuing another ZQCL or ZQCS command) can be performed on the DRAM channel by the controller for the duration of tZQinit or tZQoper. The quiet time on the DRAM channel helps accurately calibrate RON and ODT. After DRAM calibration is achieved, the DRAM should disable the ZQ ball's current consumption path to reduce power.

ZQ CALIBRATION commands can be issued in parallel to DLL RESET and locking time. Upon self refresh exit, an explicit ZQCL is required if ZQ calibration is desired.

In dual-rank systems that share the ZQ resistor between devices, the controller must not enable overlap of tZQinit, tZQoper, or tZQCS between ranks.

Figure 52 : ZQ CALIBRATION Timing (ZQCL and ZQCS)



Notes :
1. CKE must be continuously registered HIGH during the calibration procedure.
2. ODT must be disabled via the ODT signal or the MRS during the calibration procedure.
3. All devices connected to the DQ bus should be High-Z during calibration.

ACTIVATE Operation

Before any READ or WRITE commands can be issued to a bank within the DRAM, a row in that bank must be opened (activated). This is accomplished via the ACTIVATE command, which selects both the bank and the row to be activated.

After a row is opened with an ACTIVATE command, a READ or WRITE command may be issued to that row, subject to the tRCD specification. However, if the additive latency is programmed correctly, a READ or WRITE command may be issued prior to tRCD (MIN). In this operation, the DRAM enables a READ or WRITE command to be issued after the ACTIVATE command for that bank, but prior to tRCD (MIN) with the requirement that (ACTIVATE-to-READ/WRITE) + AL ≥ tRCD (MIN) (see Posted CAS Additive Latency). tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVATE command on which a READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles.

When at least one bank is open, any READ-to-READ command delay or WRITE-to-WRITE command delay is restricted to tCCD (MIN). A subsequent ACTIVATE command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVATE commands to the same bank is defined by tRC.

A subsequent ACTIVATE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVATE commands to different banks is defined by tRRD. No more than four bank ACTIVATE commands may be issued in a given tFAW (MIN) period, and the tRRD (MIN) restriction still applies. The tFAW (MIN) parameter applies, regardless of the number of banks already opened or closed.

Figure 53 : Example: Meeting tRRD (MIN) and tRCD (MIN)

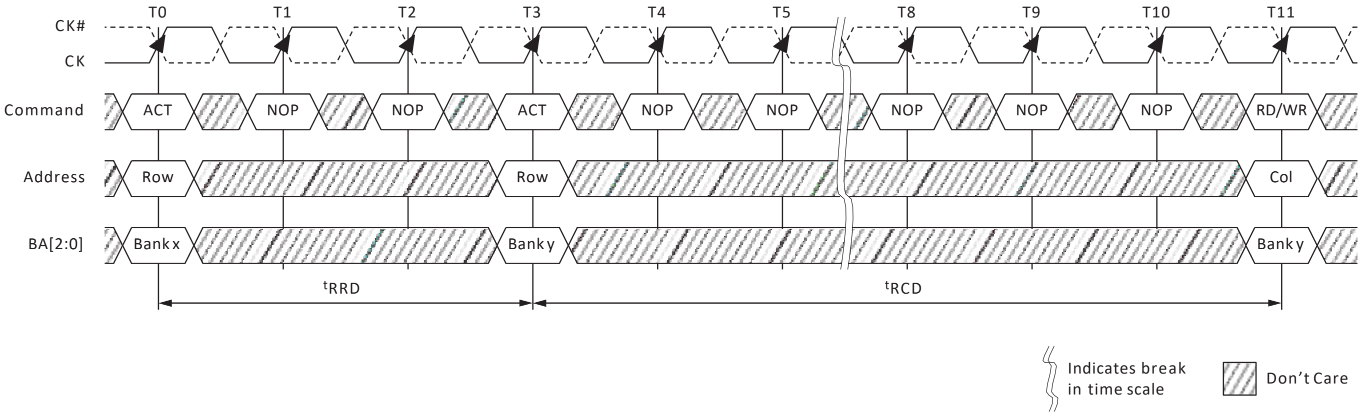
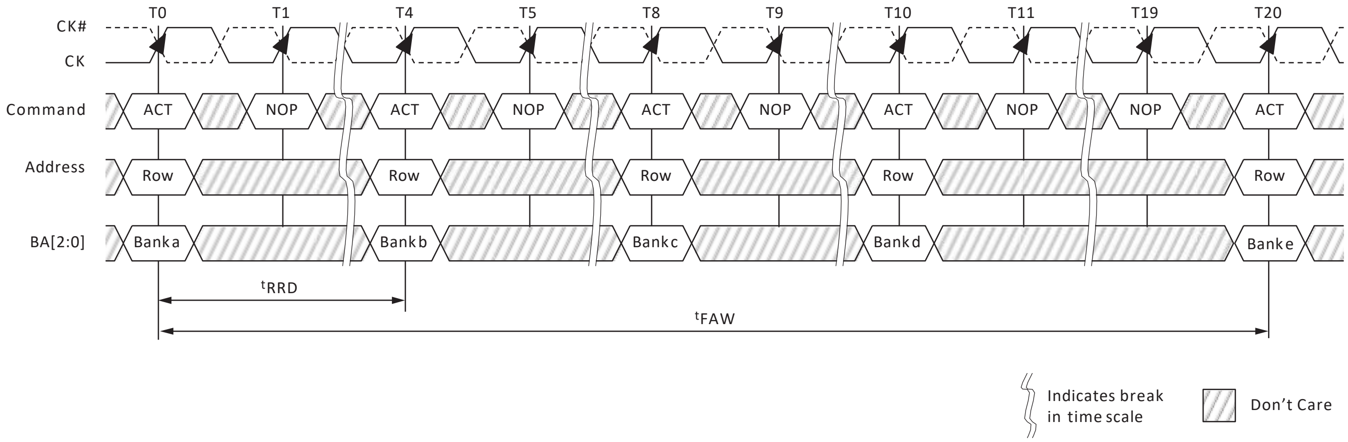


Figure 54 : Example: tFAW

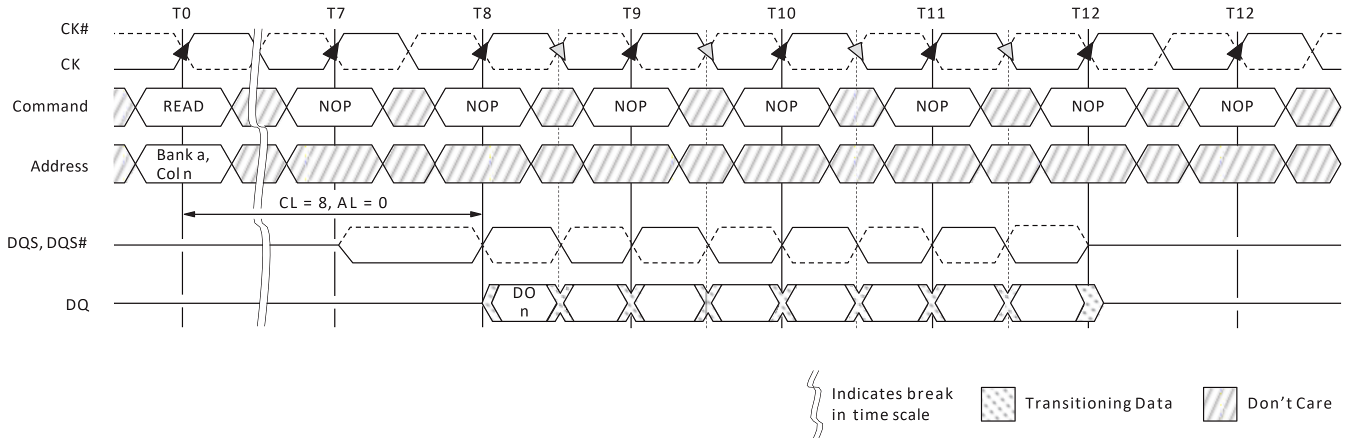


READ Operation

READ bursts are initiated with a READ command. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is automatically precharged at the completion of the burst. If auto precharge is disabled, the row will be left open after the completion of the burst.

During READ bursts, the valid data-out element from the starting column address is available READ latency (RL) clocks later. RL is defined as the sum of posted CAS additive latency (AL) and CAS latency (CL) (RL = AL + CL). The value of AL and CL is programmable in the mode register via the MRS command. Each subsequent data-out element is valid nominally at the next positive or negative clock edge (that is, at the next crossing of CK and CK#). Figure 55 shows an example of RL based on a CL setting of 8 and an AL setting of 0.

Figure 55 : READ Latency



Notes : 1. DO *n* = data-out from column *n*.
2. Subsequent elements of data-out appear in the programmed order following DO *n*.

DQS, DQS# is driven by the DRAM along with the output data. The initial LOW state on DQS and HIGH state on DQS# is known as the READ preamble (tRPRE). The LOW state on DQS and the HIGH state on DQS#, coincident with the last data-out element, is known as the READ postamble (tRPST). Upon completion of a burst, assuming no other commands have been initiated, the DQ goes High-Z. A detailed explanation of tDQSQ (valid data-out skew), tQH (data-out window hold), and the valid data window are depicted in Figure 66. A detailed explanation of tDQSCK (DQS transition skew to CK) is also depicted in Figure 66.

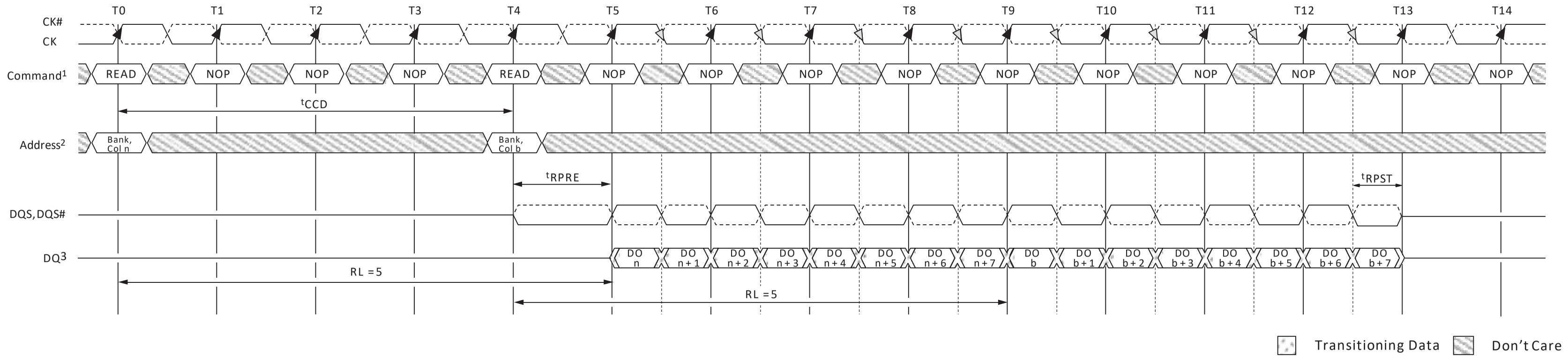
Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued tCCD cycles after the first READ command. This is shown for BL8 in Figure 56. If BC4 is enabled, tCCD must still be met, which will cause a gap in the data output, as shown in Figure 57. Nonconsecutive READ data is reflected in Figure 58. DDR3 SDRAM does not allow interrupting or truncating any READ burst.

Data from any READ burst must be completed before a subsequent WRITE burst is allowed. An example of a READ burst followed by a WRITE burst for BL8 is shown in Figure 59 (BC4 is shown in Figure 60. To ensure the READ data is completed before the WRITE data is on the bus, the minimum READ-to-WRITE timing is RL+tCCD-WL+2tCK.

A READ burst may be followed by a PRECHARGE command to the same bank, provided auto precharge is not activated. The minimum READ-to-PRECHARGE command spacing to the same bank is four clocks and must also satisfy a minimum analog time from the READ command. This time is called tRTP (READ-to-RECHARGE). tRTP starts AL cycles later than the READ command. Examples for BL8 are shown in Figure 61 and BC4 in Figure 62. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. The PRECHARGE command followed by another PRECHARGE command to the same bank is allowed. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

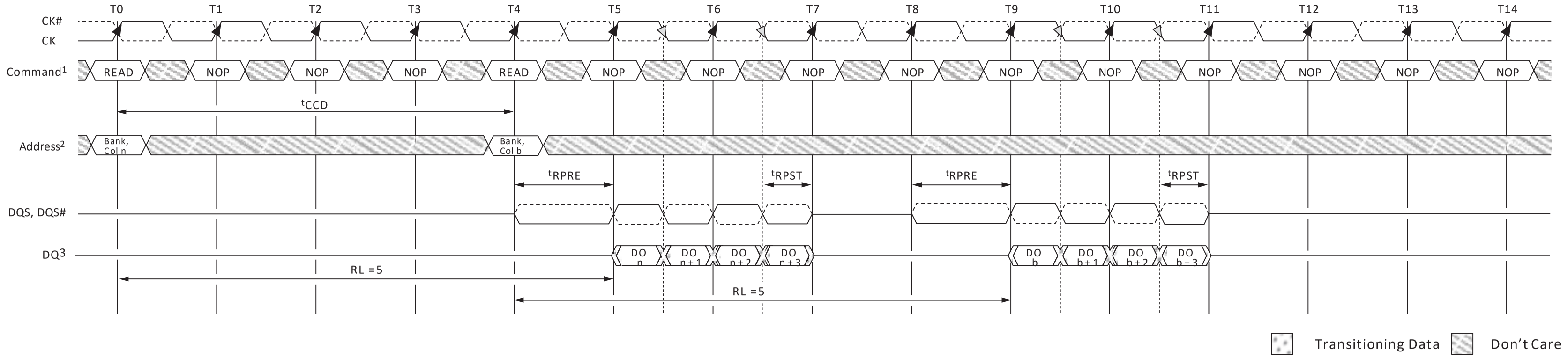
If A10 is HIGH when a READ command is issued, the READ with auto precharge function is engaged. The DRAM starts an auto precharge operation on the rising edge, which is AL + tRTP cycles after the READ command. DRAM support a tRAS lockout feature (see Figure 64). If tRAS (MIN) is not satisfied at the edge, the starting point of the auto precharge operation will be delayed until tRAS (MIN) is satisfied. If tRTP (MIN) is not satisfied at the edge, the starting point of the auto precharge operation is delayed until tRTP (MIN) is satisfied. In case the internal precharge is pushed out by tRTP, tRP starts at the point at which the internal precharge happens (not at the next rising clock edge after this event). The time from READ with auto precharge to the next ACTIVATE command to the same bank is AL + (tRTP + tRP)*, where * means rounded up to the next integer. In any event, internal precharge does not start earlier than four clocks after the last 8*n*-bit prefetch.

Figure 56 : Consecutive READ Bursts (BL8)



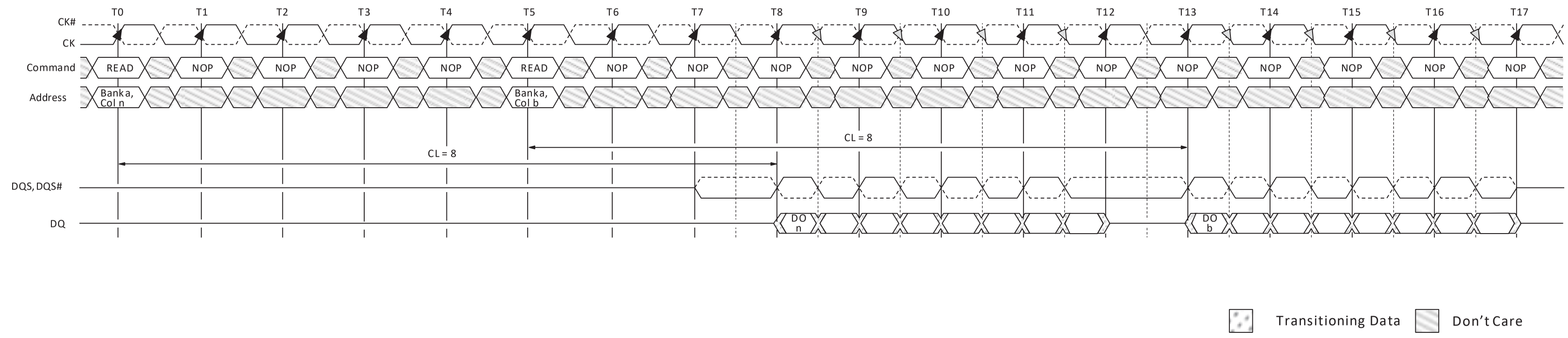
Notes : 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ command at T0 and T4.
3. DO *n* (or *b*) = data-out from column *n* (or column *b*).
4. BL8, RL = 5 (CL = 5, AL = 0).

Figure 57 : Consecutive READ Bursts (BC4)



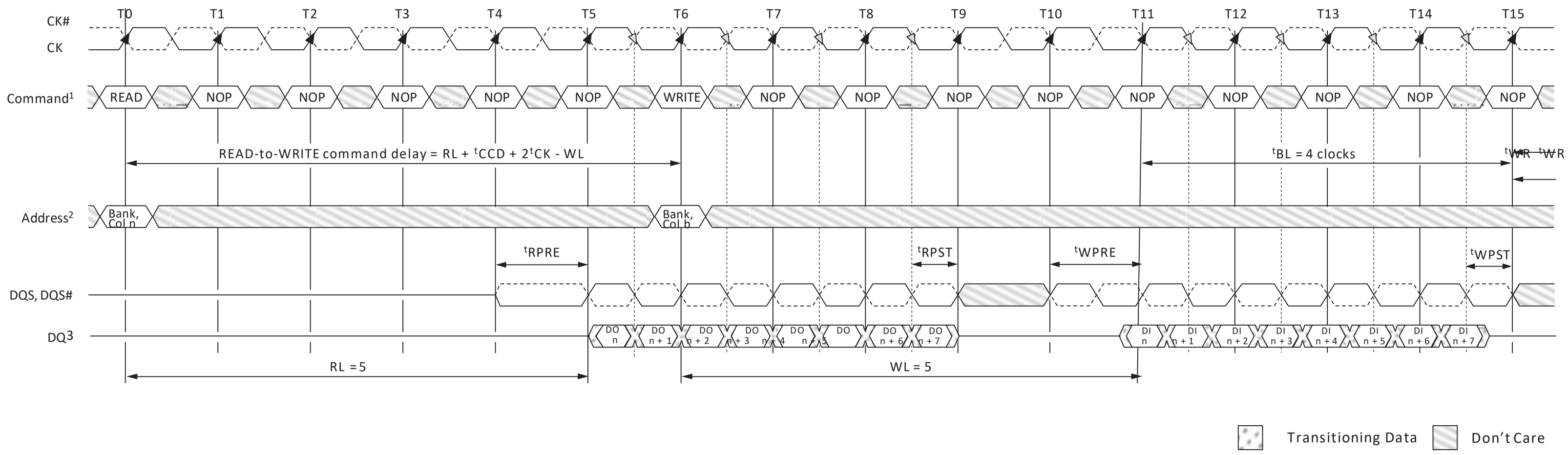
Notes : 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BC4 setting is activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ command at T0 and T4.
3. DO *n* (or *b*) = data-out from column *n* (or column *b*).
4. BC4, RL = 5 (CL = 5, AL = 0).

Figure 58 : Nonconsecutive READ Bursts



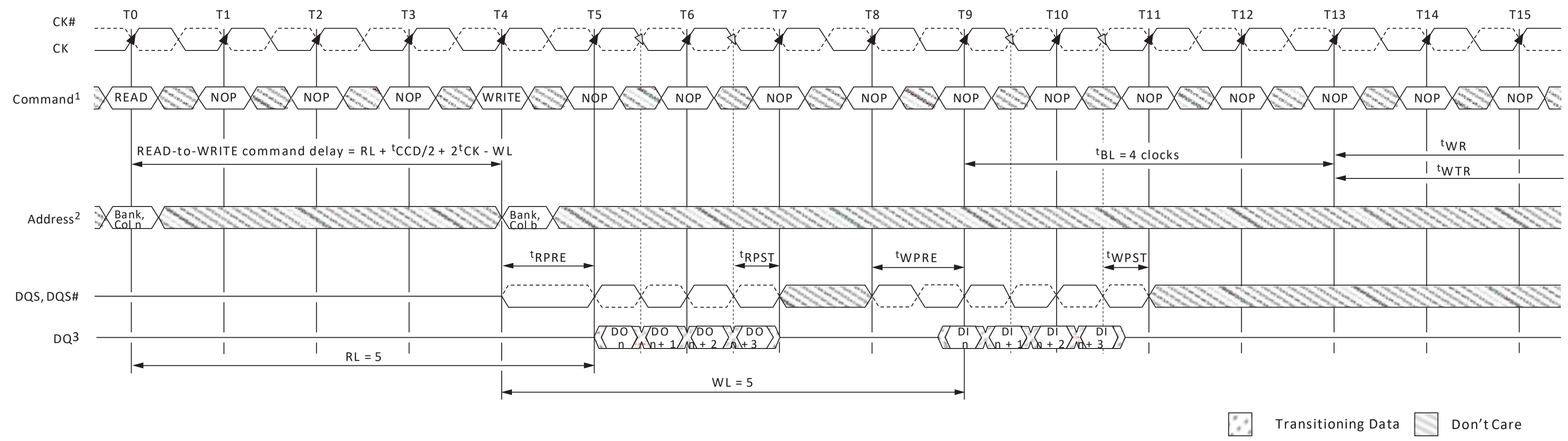
Notes : 1. AL = 0, RL = 8.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. Seven subsequent elements of data-out appear in the programmed order following DO *n*.
4. Seven subsequent elements of data-out appear in the programmed order following DO *b*.

Figure 59 : READ (BL8) to WRITE (BL8)



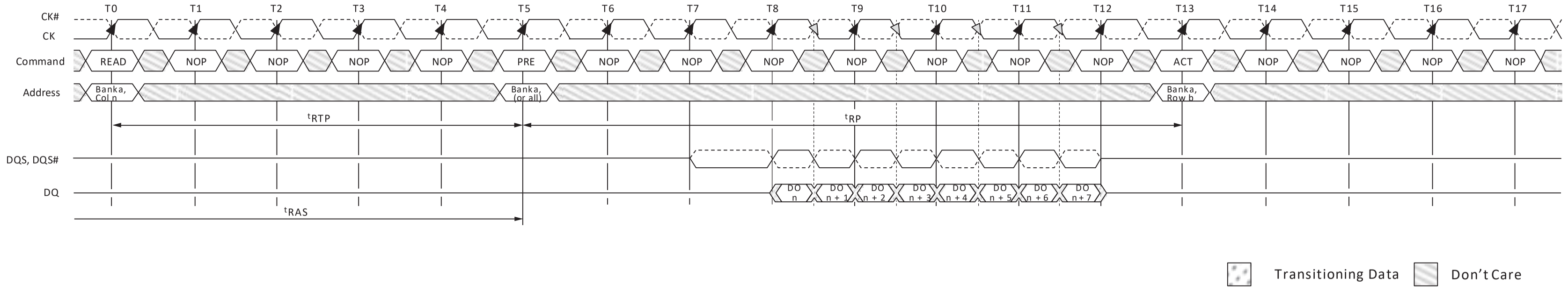
Notes : 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the READ command at T0, and the WRITE command at T6.
3. DO *n* = data-out from column, DI *b* = data-in for column *b*.
4. BL8, RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

Figure 60 : READ (BC4) to WRITE (BC4) OTF



Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BC4 OTF setting is activated by MR0[1:0] and A12 = 0 during READ command at T0 and WRITE command at T4.
3. DO *n* = data-out from column *n*; DI *n* = data-in from column *b*.
4. BC4, RL = 5 (AL - 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

Figure 61 : READ to PRECHARGE (BL8)



Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BC4 OTF setting is activated by MR0[1:0] and A12 = 0 during READ command at T0 and WRITE command at T4.
3. DO *n* = data-out from column *n*; DI *n* = data-in from column *b*.
4. BC4, RL = 5 (AL - 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

Figure 62 : READ to PRECHARGE (BC4)

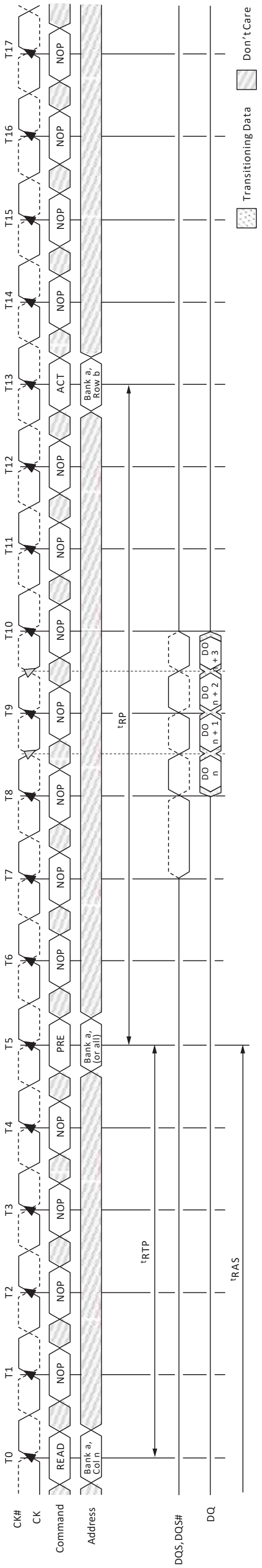


Figure 63 : READ to PRECHARGE (AL = 5, CL = 6)

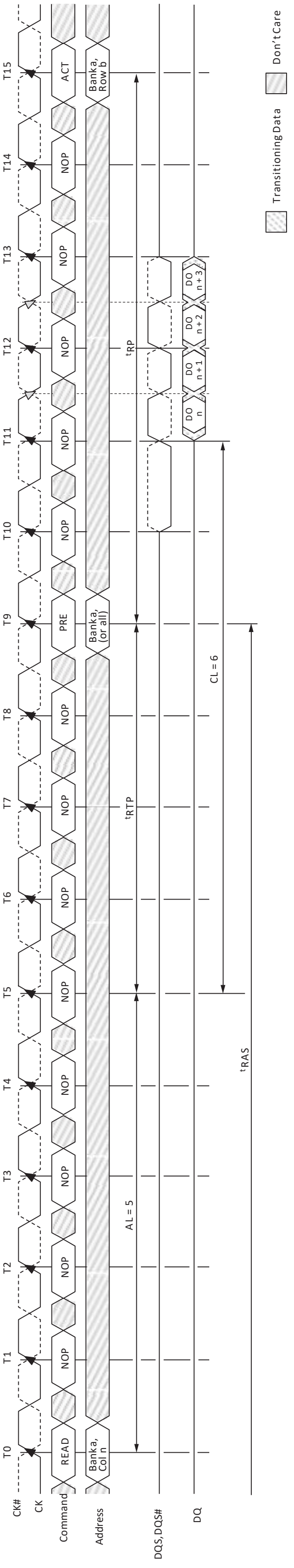
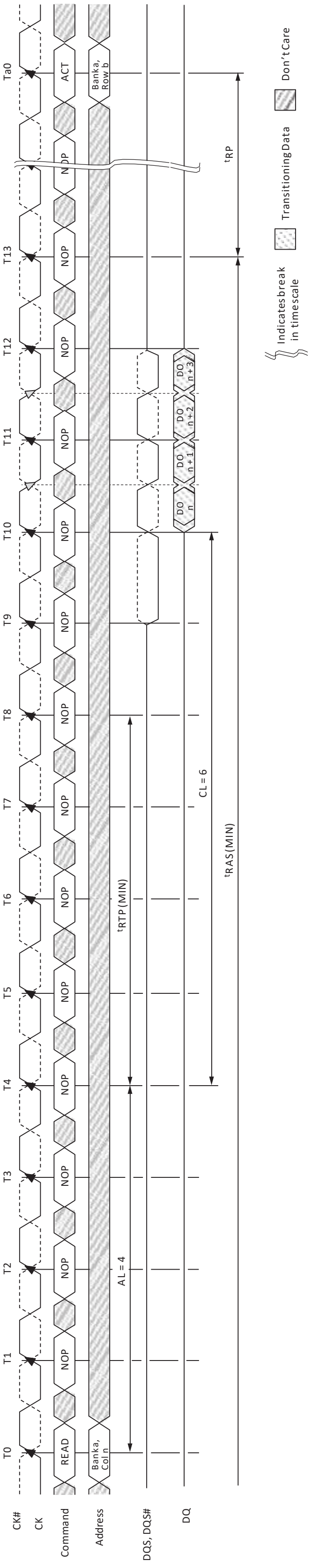


Figure 64 : READ with Auto Precharge (AL = 4, CL = 6)



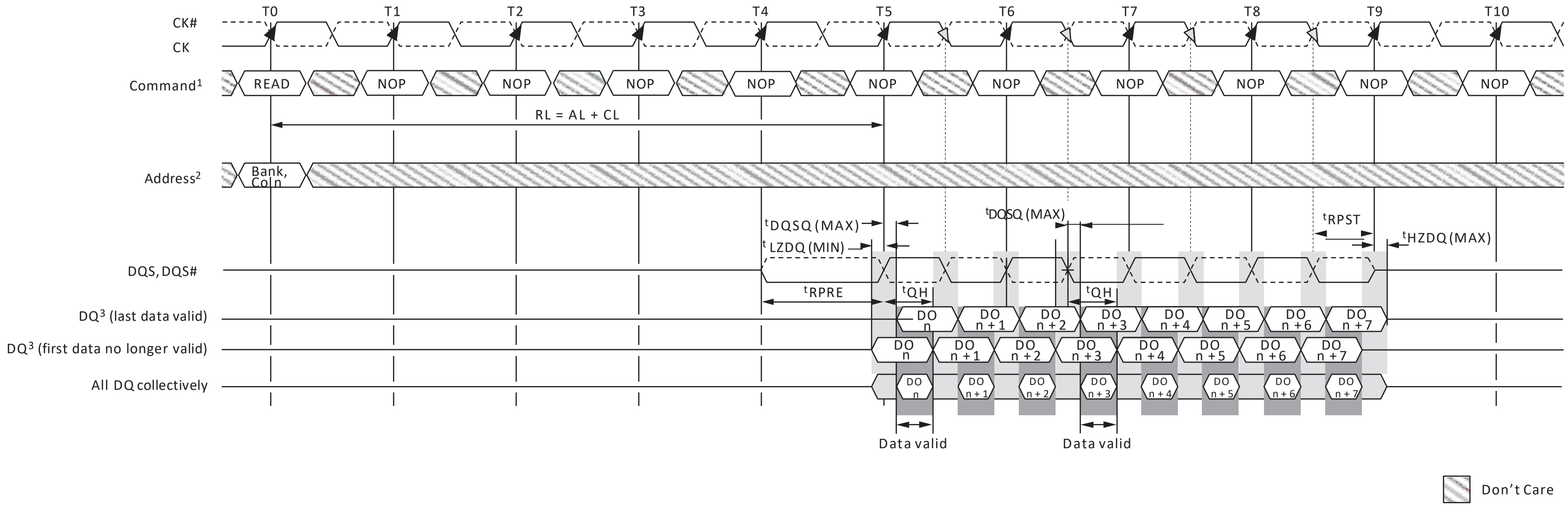
DQS to DQ output timing is shown in Figure 65. The DQ transitions between valid data outputs must be within tDQSQ of the crossing point of DQS, DQS#. DQS must also maintain a minimum HIGH and LOW time of tQSH and tQSL. Prior to the READ preamble, the DQ balls will either be floating or terminated, depending on the status of the ODT signal.

Figure 66 shows the strobe-to-clock timing during a READ. The crossing point DQS, DQS# must transition within±tDQSCK of the clock crossing point. The data out has no timing relationship to CK, only to DQS, as shown in Figure 66.

Figure 66 also shows the READ preamble and postamble. Typically, both DQS and DQS# are High-Z to save power (VDDQ). Prior to data output from the DRAM, DQS is driven LOW and DQS# is HIGH for tRPRE. This is known as the READ preamble.

The READ postamble, tRPST, is one half clock from the last DQS, DQS# transition. During the READ postamble, DQS is driven LOW and DQS# is HIGH. When complete, the DQ is disabled or continues terminating, depending on the state of the ODT signal. On page demonstrates how to measure tRPST.

Figure 65 : Data Output Timing – tDQSQ and Data Valid Window



Notes : 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.

2. The BL8 setting is activated by either MR0[1, 0] = 0, 0 or MR0[0, 1] = 0, 1 and A12 = 1 during READ command at T0.

3. DO *n* = data-out from column *n*.

4. BL8, RL = 5 (AL = 0, CL = 5).

5. Output timings are referenced to VDDQ/2 and DLL on and locked.

6. tDQSQ defines the skew between DQS, DQS# to data and does not define DQS, DQS# to CK.

7. Early data transitions may not always happen at the same DQ. Data transitions of a DQ can be early or late within a burst.

tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZDQS and tHZDQ, or begins driving tLZDQS, tLZDQ. Figure 67 shows a method of calculating the point when the device is no longer driving tHZDQS and tHZDQ, or begins driving tLZDQS, tLZDQ, by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZDQS, tLZDQ, tHZDQS, and tHZDQ are defined as single-ended.

Figure 66 : Data Strobe Timing – READs

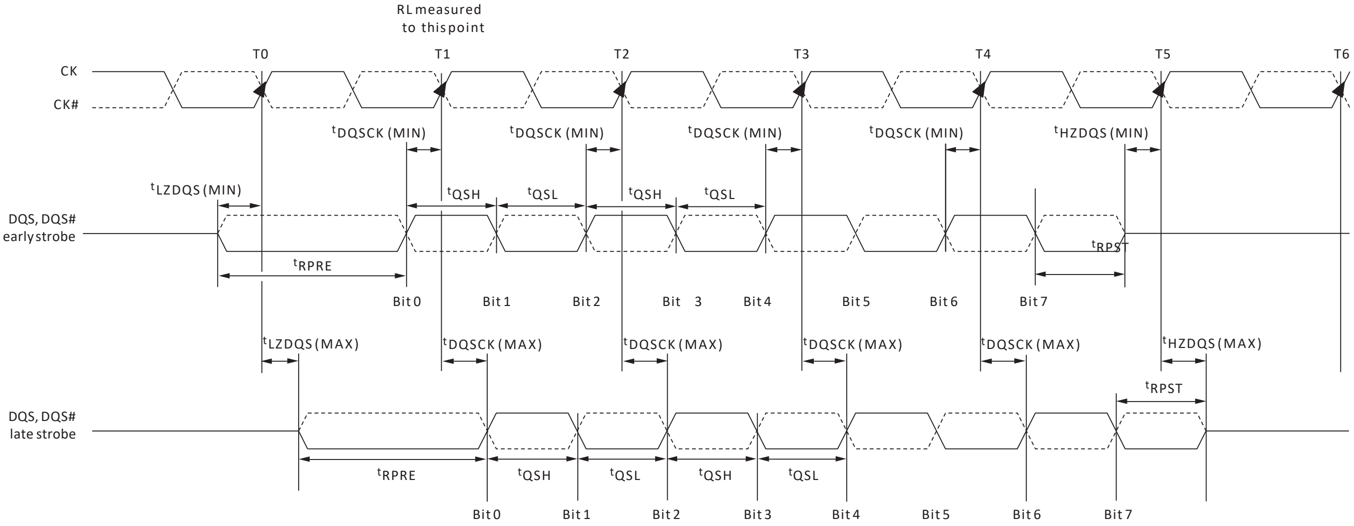
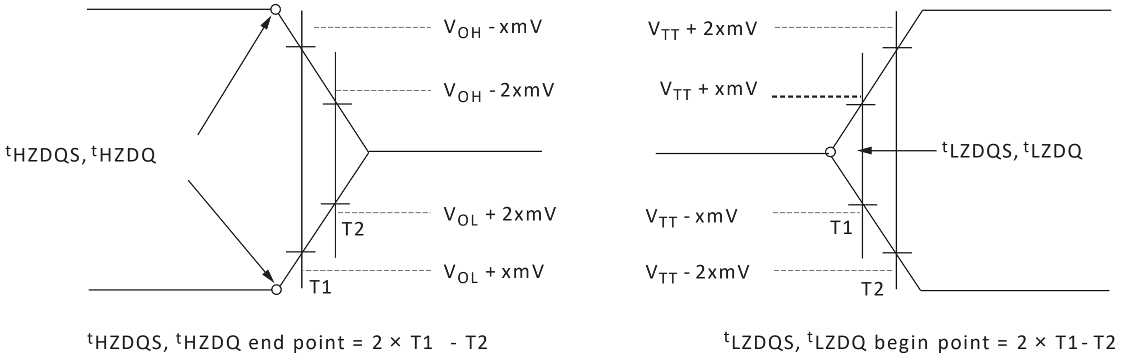


Figure 67 : Method for Calculating tLZ and tHZ



Notes :
1. Within a burst, the rising strobe edge is not necessarily fixed at tDQSCK (MIN) or tDQSCK (MAX). Instead, the rising strobe edge can vary between tDQSCK (MIN) and tDQSCK (MAX).
2. The DQS HIGH pulse width is defined by tQSH, and the DQS LOW pulse width is defined by tQSL. Likewise, tLZDQS (MIN) and tHZDQS (MIN) are not tied to tDQSCK (MIN) (early strobe case), and tLZDQS (MAX) and tHZDQS (MAX) are not tied to tDQSCK (MAX) (late strobe case); however, they tend to track one another.
3. The minimum pulse width of the READ preamble is defined by tRPRE (MIN). The minimum pulse width of the READ postamble is defined by tRPST (MIN).

Figure 68 : tRPRE Timing

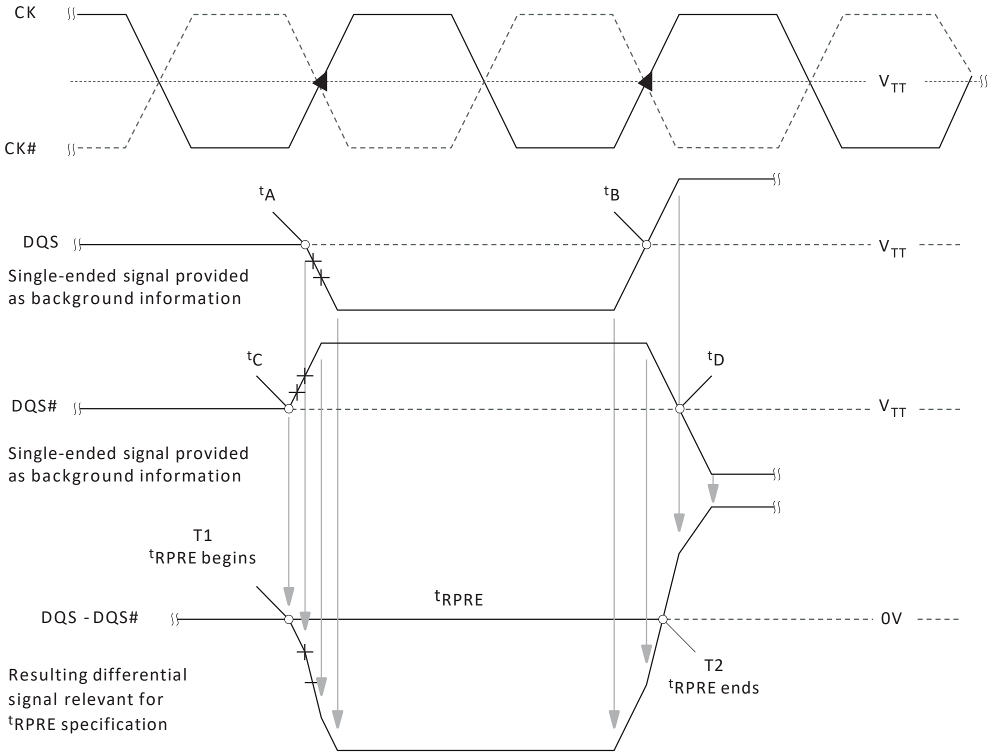
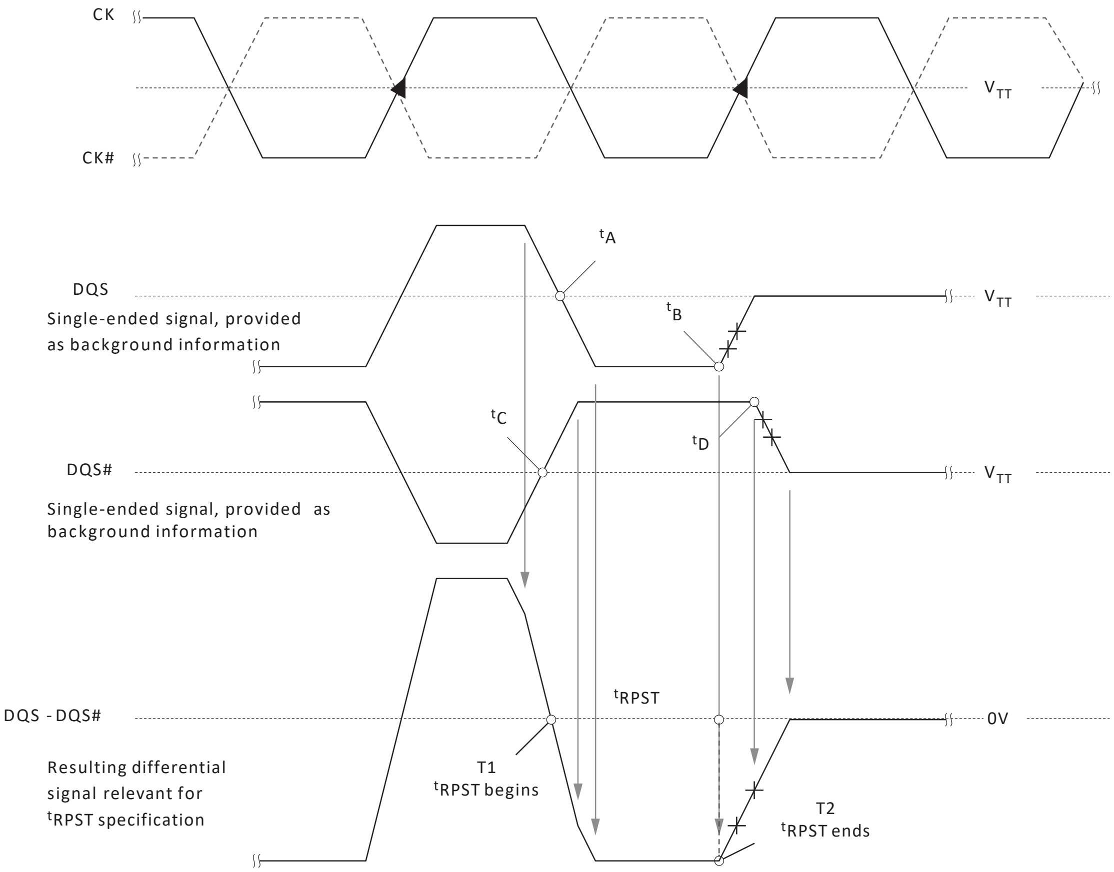


Figure 69 : tRPST Timing



WRITE Operation

WRITE bursts are initiated with a WRITE command. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is selected, the row being accessed is precharged at the end of the WRITE burst. If auto precharge is not selected, the row will remain open for subsequent accesses. After a WRITE command has been issued, the WRITE burst may not be interrupted. For the generic WRITE commands used in Figure 72 through Figure 80, auto precharge is disabled.

During WRITE bursts, the first valid data-in element is registered on a rising edge of DQS following the WRITE latency (WL) clocks later and subsequent data elements will be registered on successive edges of DQS. WRITE latency (WL) is defined as the sum of posted CAS additive latency (AL) and CAS WRITE latency (CWL): WL=AL+CWL. The values of AL and CWL are programmed in the MR0 and MR2 registers, respectively. Prior to the first valid DQS edge, a full cycle is needed (including a dummy crossover of DQS(#)) and specified as the WRITE preamble shown in Figure 72. The half cycle on DQS following the last data-in element is known as the WRITE postamble.

The time between the WRITE command and the first valid edge of DQS is WL clocks ±tDQSS. Figure 73 through Figure 80 show the nominal case where tDQSS = 0ns; however, Figure 72 includes tDQSS (MIN) and tDQSS (MAX) cases.

Data may be masked from completing a WRITE using data mask. The data mask occurs on the DM ball aligned to the WRITE data. If DM is LOW, the WRITE completes normally. If DM is HIGH, that bit of data is masked.

Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z, and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with a subsequent WRITE command to provide a continuous flow of input data. The new WRITE command can be tCCD clocks following the previous WRITE command. The first data element from the new burst is applied after the last element of a completed burst. Figure 73 and Figure 74 show concatenated bursts. An example of nonconsecutive WRITEs is shown in Figure 75.

Data for any WRITE burst may be followed by a subsequent READ command after tWTR has been met (see Figure 76, Figure 77, and Figure 78).

Data for any WRITE burst may be followed by a subsequent PRECHARGE command, providing tWR has been met, as shown in Figure 79 and Figure 80.

Both tWTR and tWR starting time may vary, depending on the mode register settings (fixed BC4, BL8 versus OTF).

Figure 70 : tWPRE Timing

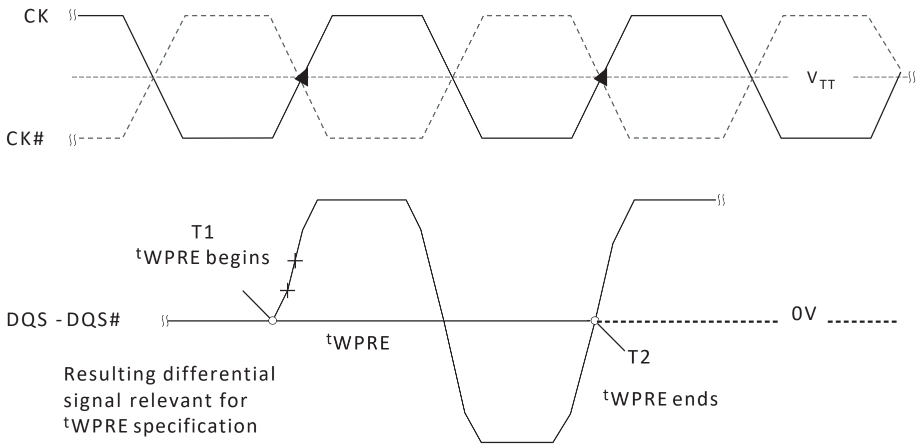


Figure 71 : tWPST Timing

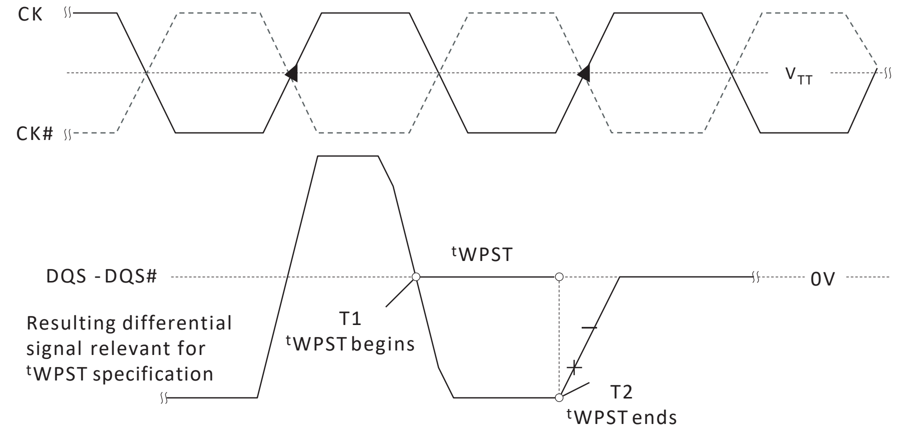
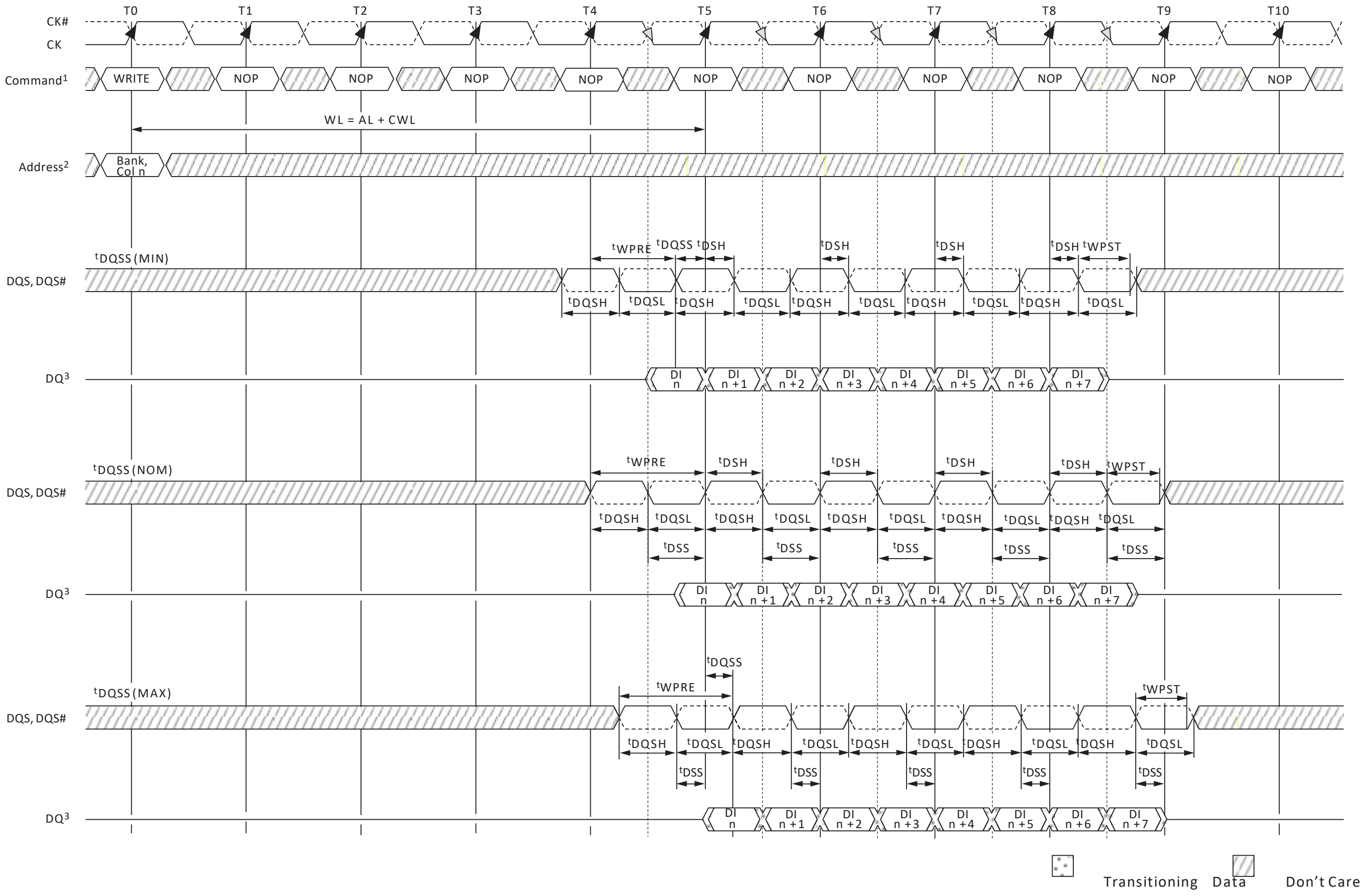
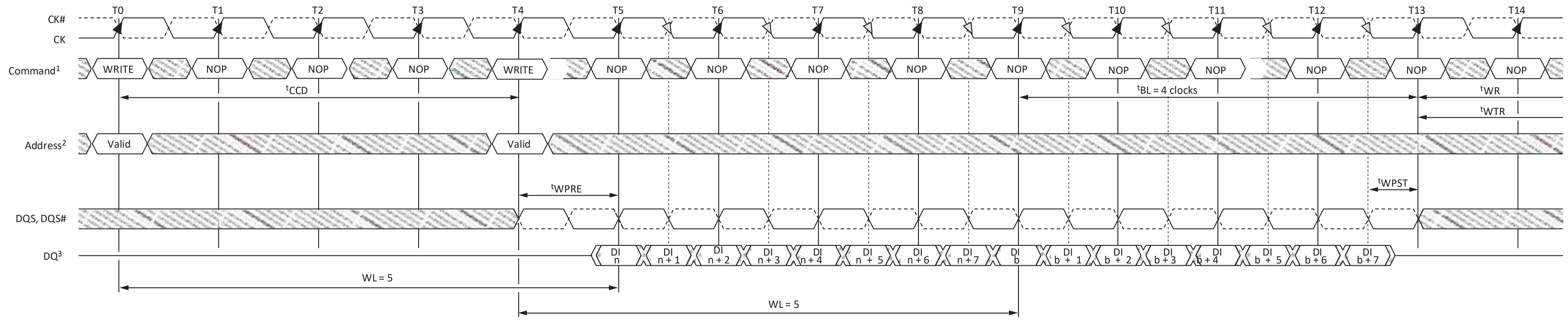


Figure 72 : WRITE Burst



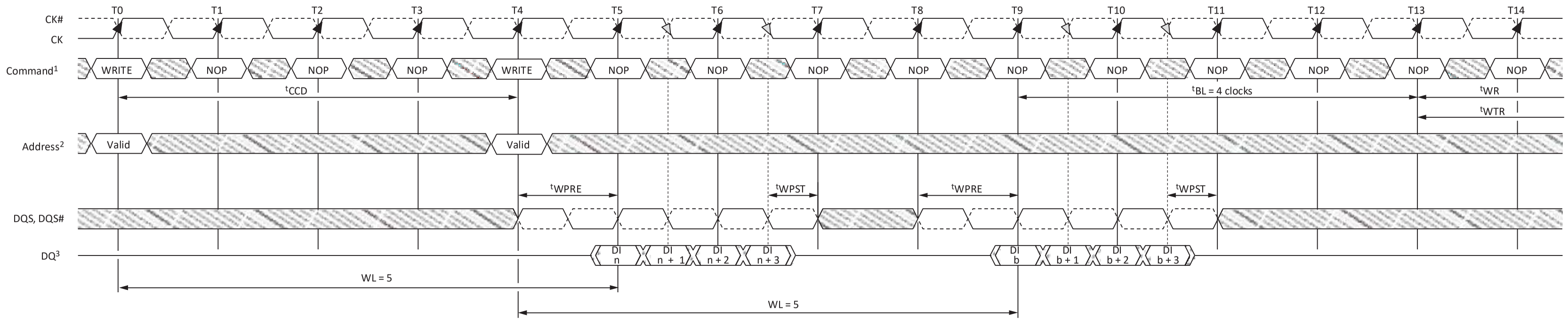
Notes :
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the WRITE command at T0.
3. DI *n* = data-in for column *n*.
4. BL8, WL = 5 (AL = 0, CWL = 5).
5. tDQSS must be met at each rising clock edge.
6. tWPST is usually depicted as ending at the crossing of DQS, DQS#; however, tWPST actually ends when DQS no longer drives LOW and DQS# no longer drives HIGH.

Figure 73 : Consecutive WRITE (BL8) to WRITE (BL8)



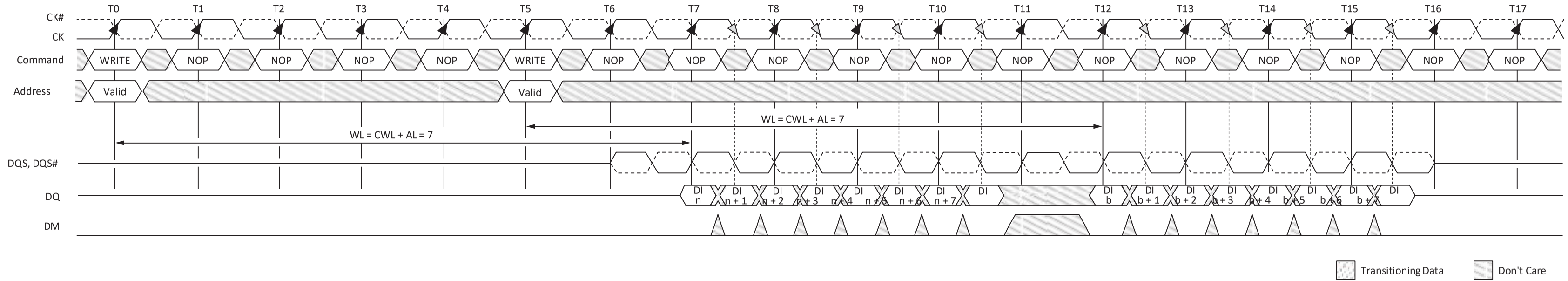
Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the WRITE commands at T0 and T4.
3. DI *n* (or *b*) = data-in for column *n* (or column *b*).
4. BL8, WL = 5 (AL = 0, CWL = 5).

Figure 74 : Consecutive WRITE (BC4) to WRITE (BC4) via OTF



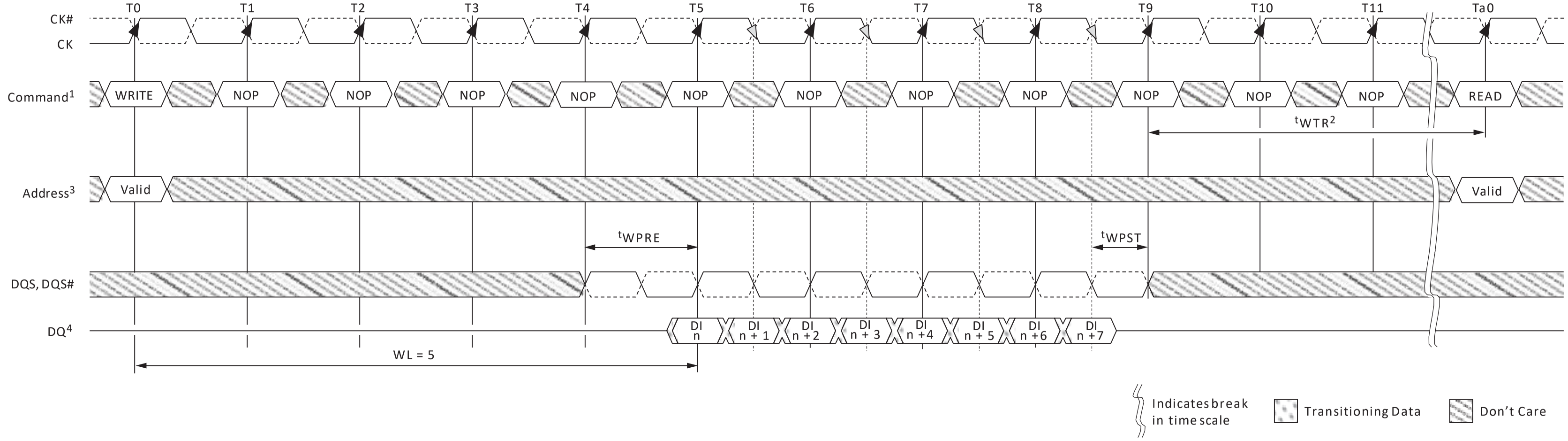
Notes:1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BC4, WL = 5 (AL = 0, CWL = 5).
3. DI *n* (or *b*) = data-in for column *n* (or column *b*).
4. The BC4 setting is activated by MR0[1:0] = 01 and A12 = 0 during the WRITE command at T0 and T4.
5. If set via MRS (fixed) tWR and tWTR would start T11 (2 cycles earlier).

Figure 75 : Nonconsecutive WRITE to WRITE



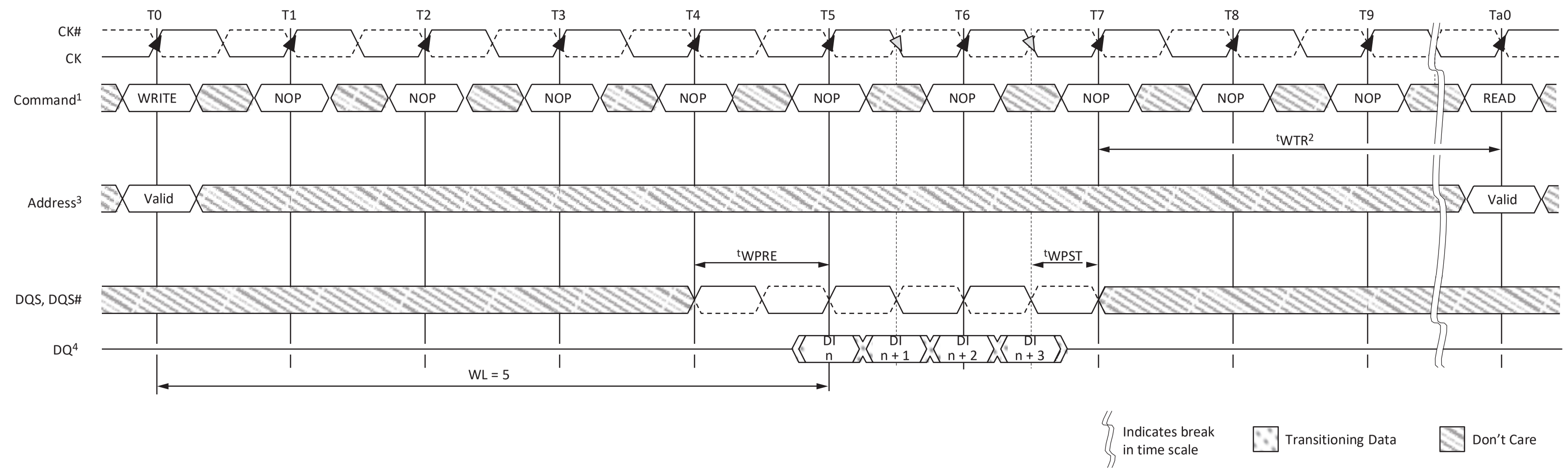
Notes: 1. DI *n* (or *b*) = data-in for column *n* (or column *b*).
2. Seven subsequent elements of data-in are applied in the programmed order following DO *n*.
3. Each WRITE command may be to any bank.
4. Shown for WL = 7 (CWL = 7, AL = 0).

Figure 76 : Nonconsecutive WRITE to WRITE



Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. tWTR controls the WRITE-to-READ delay to the same device and starts with the first rising clock edge after the last write data shown at T9.
3. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and MR0[12] = 1 during the WRITE command at T0. The READ command at Ta0 can be either BC4 or BL8, depending on MR0[1:0] and the A12 status at Ta0.
4. DI *n* = data-in for column *n*.
5. RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

Figure 77 : WRITE to READ (BC4 Mode Register Setting)



Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.

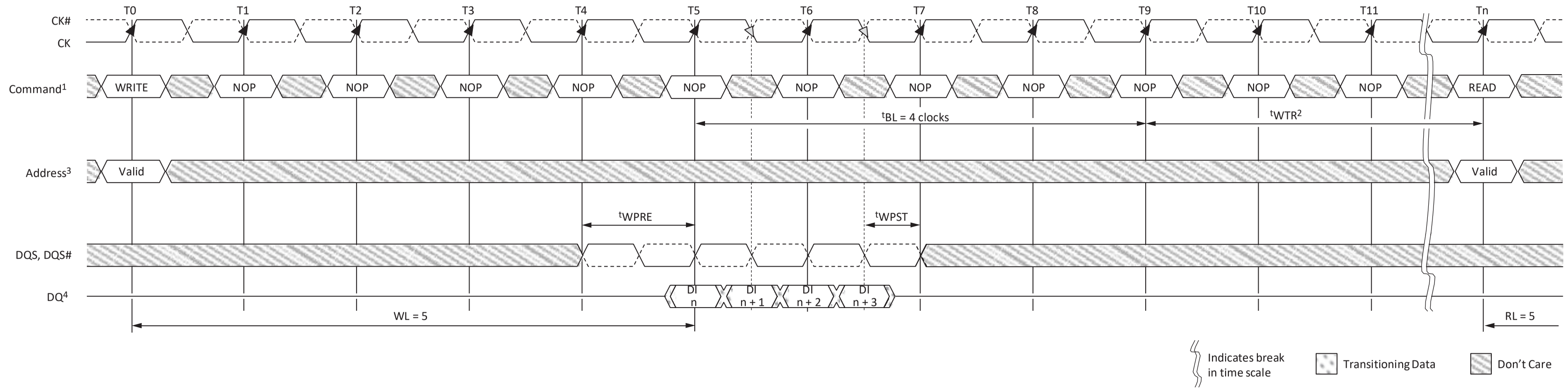
2. tWTR controls the WRITE-to-READ delay to the same device and starts with the first rising clock edge after the last write data shown at T7.

3. The fixed BC4 setting is activated by MR0[1:0] = 10 during the WRITE command at T0 and the READ command at Ta0.

4. DI *n* = data-in for column *n*.

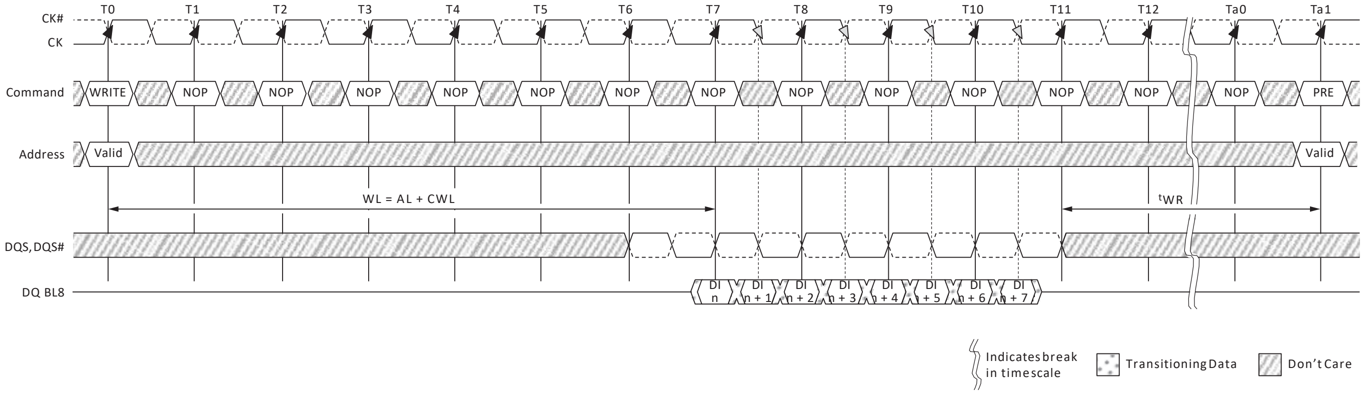
5. BC4 (fixed), WL = 5 (AL = 0, CWL = 5), RL = 5 (AL = 0, CL = 5).

Figure 78 : WRITE (BC4 OTF) to READ (BC4 OTF)



Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. tWTR controls the WRITE-to-READ delay to the same device and starts after tBL.
3. The BC4 OTF setting is activated by MR0[1:0] = 01 and A12 = 0 during the WRITE command at T0 and the READ command at T*n*.
4. DI *n* = data-in for column *n*.
5. BC4, RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

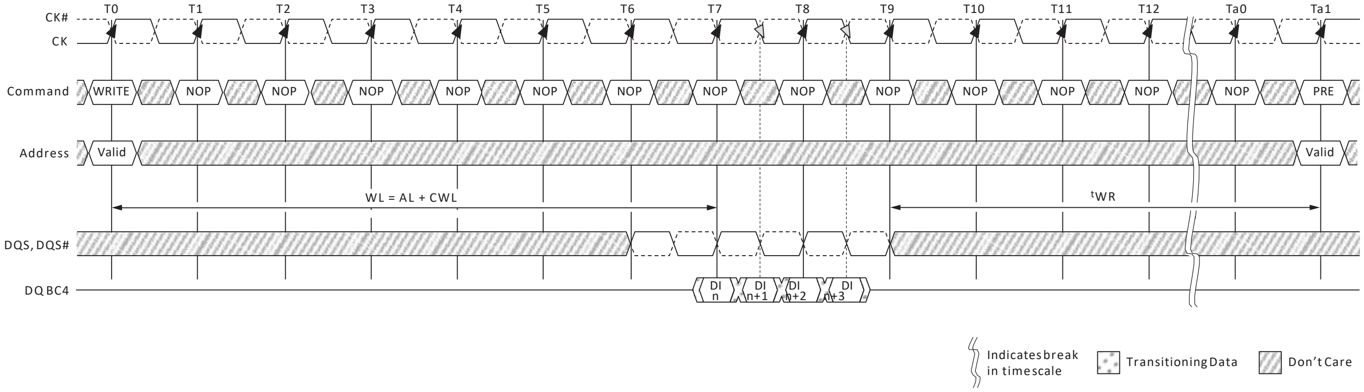
Figure 79 : WRITE (BL8) to PRECHARGE



Notes: 1. DI *n* = data-in from column *n*.

2. Seven subsequent elements of data-in are applied in the programmed order following DO *n*.
3. Shown for WL = 7 (AL = 0, CWL = 7).

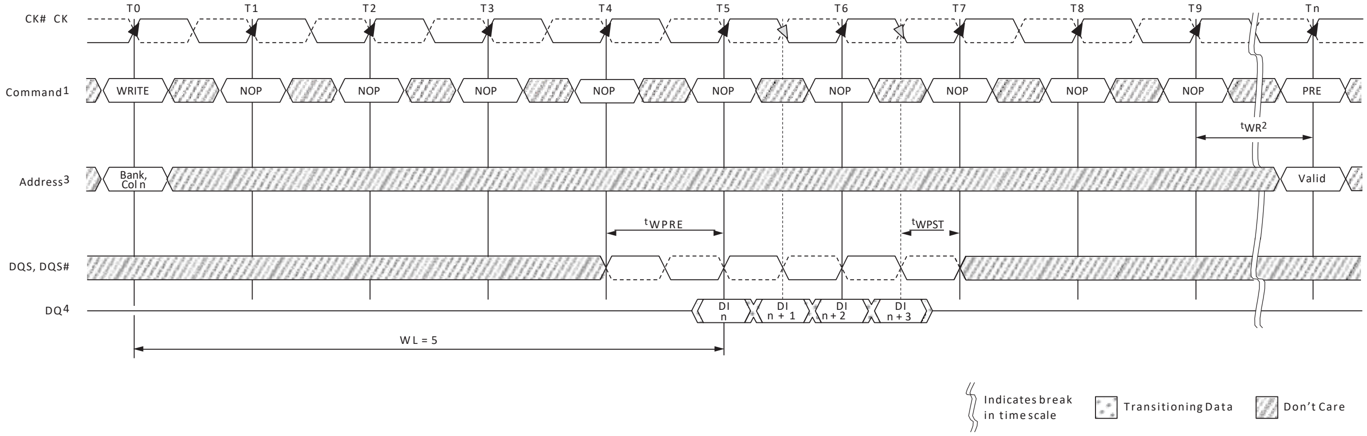
Figure 80 : WRITE (BC4 Mode Register Setting) to PRECHARGE



Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.

2. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data is shown at T7. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.
3. The fixed BC4 setting is activated by MR0[1:0] = 10 during the WRITE command at T0.
4. DI *n* = data-in for column *n*.
5. BC4 (fixed), WL = 5, RL = 5.

Figure 81 : WRITE (BC4 OTF) to PRECHARGE



Notes: 1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The write recovery time (tWR) is referenced from the rising clock edge at T9. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.
3. The BC4 setting is activated by MR0[1:0] = 01 and A12 = 0 during the WRITE command at T0.
4. DI *n* = data-in for column *n*.
5. BC4 (OTF), WL = 5, RL = 5.

DQ Input Timing

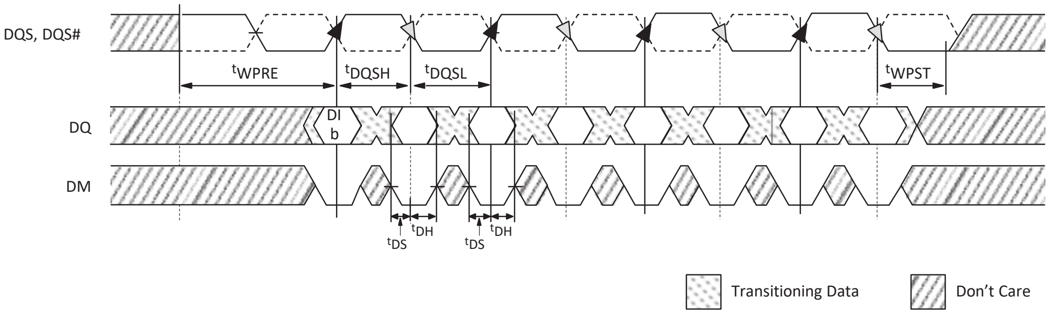
Figure 72 shows the strobe-to-clock timing during a WRITE burst. DQS, DQS# must transition within 0.25tCK of the clock transitions, as limited by tDQSS. All data and data mask setup and hold timings are measured relative to the DQS, DQS# crossing, not the clock crossing.

The WRITE preamble and postamble are also shown in Figure 72. One clock prior to data input to the DRAM, DQS must be HIGH and DQS# must be LOW. Then for a half clock, DQS is driven LOW (DQS# is driven HIGH) during the WRITE preamble, tWPRE. Likewise, DQS must be kept LOW by the controller after the last data is written to the DRAM during the WRITE postamble, tWPST.

Data setup and hold times are also shown in Figure 72. All setup and hold times are measured from the crossing points of DQS and DQS#. These setup and hold values pertain to data input and data mask input.

Additionally, the half period of the data input strobe is specified by tDQSH and tDQSL.

Figure 82 : Data Input Timing



PRECHARGE Operation

Input A10 determines whether one bank or all banks are to be precharged and, in the case where only one bank is to be precharged, inputs BA[2:0] select the bank.

When all banks are to be precharged, inputs BA[2:0] are treated as “Don’t Care.” After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued.

SELF REFRESH Operation

The SELF REFRESH operation is initiated like a REFRESH command except CKE is LOW.
The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled and reset upon exiting SELFREFRESH.

All power supply inputs (including VREFCA and VREFDQ) must be maintained at valid levels upon entry/exit and during self refresh mode operation. VREFDQ may float or not drive VDDQ/2 while in self refresh mode under certain conditions :

- VSS < VREFDQ < VDD is maintained.
- VREFDQ is valid and stable prior to CKE going back HIGH.
- The first WRITE operation may not occur earlier than 512 clocks after VREFDQ is valid.
- All other self refresh mode exit timing requirements are met.

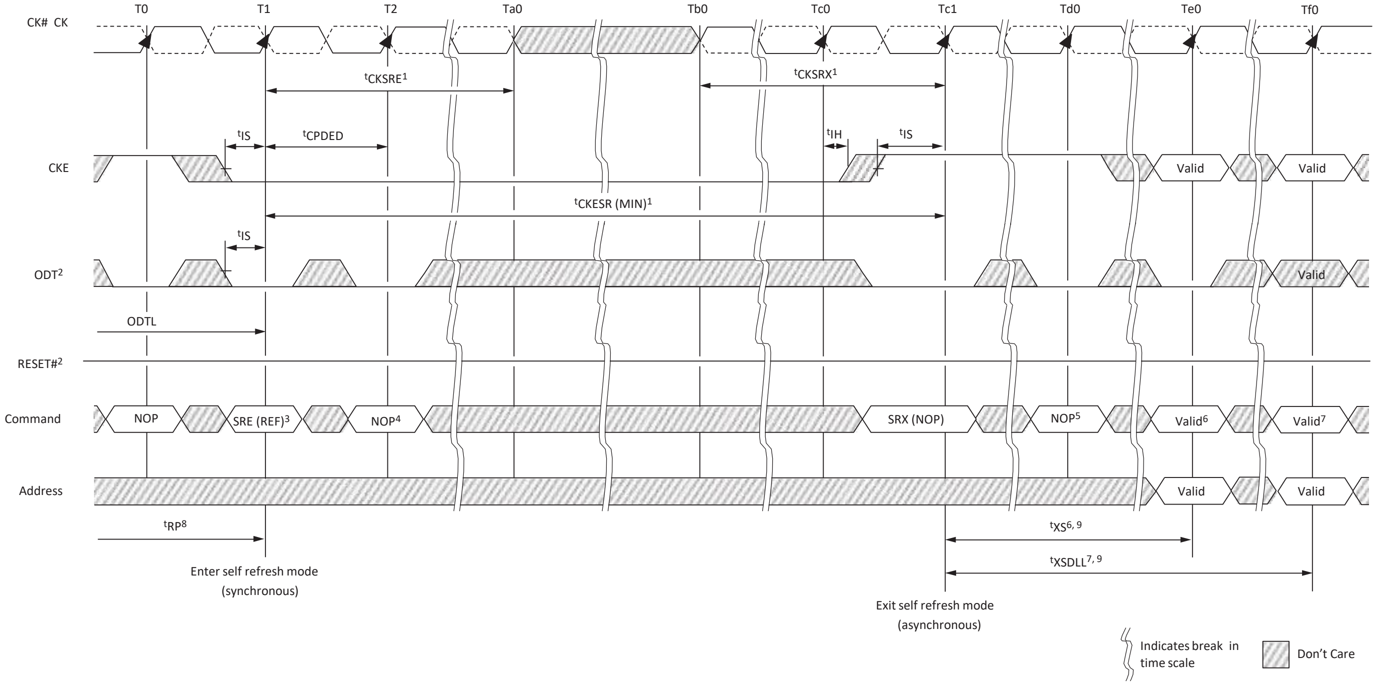
The DRAM must be idle with all banks in the precharge state (tRP is satisfied and no bursts are in progress) before a self refresh entry command can be issued. ODT must also be turned off before self refresh entry by registering the ODT ball LOW prior to the self refresh entry command (see On-Die Termination (ODT) for timing requirements). If RTT,nom and RTT(WR) are disabled in the mode registers, ODT can be a “Don’t Care.” After the self refresh entry command is registered, CKE must be held LOW to keep the DRAM in self refresh mode.

After the DRAM has entered self refresh mode, all external control signals, except CKE and RESET#, are “Don’t Care.” The DRAM initiates a minimum of one REFRESH command internally within the tCKE period when it enters self refresh mode.

The requirements for entering and exiting self refresh mode depend on the state of the clock during self refresh mode. First and foremost, the clock must be stable (meeting tCK specifications) when self refresh mode is entered. If the clock remains stable and the frequency is not altered while in self refresh mode, then the DRAM is allowed to exit self refresh mode after tCKESR is satisfied (CKE is allowed to transition HIGH tCKESR later than when CKE was registered LOW). Since the clock remains stable in self refresh mode (no frequency change), tCKSRE and tCKSRX are not required. However, if the clock is altered during self refresh mode (if it is turned-off or its frequency changes), then tCKSRE and tCKSRX must be satisfied. When entering self refresh mode, tCKSRE must be satisfied prior to altering the clock's frequency. Prior to exiting self refresh mode, tCKSRX must be satisfied prior to registering CKE HIGH.

When CKE is HIGH during self refresh exit, NOP or DES must be issued for tXS time. tXS is required for the completion of any internal refresh already in progress and must be satisfied before a valid command not requiring a locked DLL can be issued to the device. tXS is also the earliest time self refresh re-entry may occur. Before a command requiring a locked DLL can be applied, a ZQCL command must be issued, tZQOPER timing must be met, and tXSDLL must be satisfied. ODT must be off during tXSDLL.

Figure 83 : Self Refresh Entry/Exit Timing



Notes: 1. The clock must be valid and stable, meeting tCK specifications at least tCKSRE after entering self refresh mode, and at least tCKSRX prior to exiting self refresh mode, if the clock is stopped or altered between states Ta0 and Tb0. If the clock remains valid and unchanged from entry and during self refresh mode, then tCKSRE and tCKSRX do not apply; however, tCKESR must be satisfied prior to exiting at SRX.

2. ODT must be disabled and RTT off prior to entering self refresh at state T1. If both RTT,nom and RTT(WR) are disabled in the mode registers, ODT can be a "Don't Care."
3. Self refresh entry (SRE) is synchronous via a REFRESH command with CKE LOW.
4. A NOP or DES command is required at T2 after the SRE command is issued prior to the inputs becoming "Don't Care."
5. NOP or DES commands are required prior to exiting self refresh mode until state Te0.
6. tXS is required before any commands not requiring a locked DLL.
7. tXSDLL is required before any commands requiring a locked DLL.
8. The device must be in the all banks idle state prior to entering self refresh mode. For example, all banks must be precharged, tRP must be met, and no data bursts can be in progress.
9. Self refresh exit is asynchronous; however, tXS and tXSDLL timings start at the first rising clock edge where CKE HIGH satisfies tISXR at Tc1. tCKSRX timing is also measured so that tISXR is satisfied at Tc1.

Extended Temperature Usage

Dosilicon’s DDR3 SDRAM support the optional extended case temperature (TC) range of 0°C to 95°C. Thus, the SRT and ASR options must be used at a minimum.

The extended temperature range DRAM must be refreshed externally at 2x (double refresh) anytime the case temperature is above 85°C (and does not exceed 95°C). The external refresh requirement is accomplished by reducing the refresh period from 64ms to 32ms. However, self refresh mode requires either ASR or SRT to support the extended temperature. Thus, either ASR or SRT must be enabled when TC is above 85°C or self refresh cannot be used until TC is at or below 85°C. Table 73 summarizes the two extended temperature options and Table 74 summarizes how the two extended temperature options relate to one another.

Table 73 : Self Refresh Temperature and Auto Self Refresh Description

Field	MR2 Bits	Description
Self Refresh Temperature (SRT)		
SRT	7	If ASR is disabled (MR2[6] = 0), SRT must be programmed to indicate T_{OPER} during self refresh: *MR2[7] = 0: Normal operating temperature range (0°C to 85°C) *MR2[7] = 1: Extended operating temperature range (0°C to 95°C) If ASR is enabled (MR2[7] = 1), SRT must be set to 0, even if the extended temperature range is supported *MR2[7] = 0: SRT is disabled
Auto Self Refresh (ASR)		
ASR	6	When ASR is enabled, the DRAM automatically provides SELF REFRESH power management func- tions, (refresh rate for all supported operating temperature values) * MR2[6] = 1: ASR is enabled (M7 must = 0) When ASR is not enabled, the SRT bit must be programmed to indicate T_{OPER} during SELF REFRESH operation * MR2[6] = 0: ASR is disabled; must use manual self refresh temperature (SRT)

Table 74 : Self Refresh Mode Summary

MR2[6] (ASR)	MR2[7] (SRT)	SELF REFRESH Operation	Permitted Operating Temperature Range for Self Refresh Mode
0	0	Self refresh mode is supported in the normal temperature range	Normal (0°C to 85°C)
0	1	Self refresh mode is supported in normal and extended temper- ature ranges; When SRT is enabled, it increases self refresh power consumption	Normal and extended (0°C to 95°C)
1	0	Self refresh mode is supported in normal and extended temper- ature ranges; Self refresh power consumption may be tempera- ture-dependent	Normal and extended (0°C to 95°C)
1	1	Illegal	

Power-Down Mode

Power-down is synchronously entered when CKE is registered LOW coincident with a NOP or DES command. CKE is not allowed to go LOW while an MRS, MPR, ZQCAL, READ, or WRITE operation is in progress. CKE is allowed to go LOW while any of the other legal operations (such as ROW ACTIVATION, PRECHARGE, auto precharge, or REFRESH) are in progress. However, the power-down IDD specifications are not applicable until such operations have completed. Depending on the previous DRAM state and the command issued prior to CKE going LOW, certain timing constraints must be satisfied (as noted in Table 75). Timing diagrams detailing the different power-down mode entry and exits are shown in Figure 84 through Figure 93.

Table 75 : Command to Power-Down Entry Parameters

DRAM Status	Last Command Prior to CKE LOW1	Parameter (Min)	Parameter Value	Figure
Idle or active	ACTIVATE	tACTPDEN	1tCK	91
Idle or active	PRECHARGE	tPRPDEN	1tCK	92
Active	READ or READAP	tRDPDEN	RL + 4tCK + 1tCK	87
Active	WRITE: BL8OTF, BL8MRS, BC4OTF	tWRPDEN	WL + 4tCK + tWR/tCK	88
Active	WRITE: BC4MRS		WL + 2tCK + tWR/tCK	88
Active	WRITEAP: BL8OTF, BL8MRS, BC4OTF	tWRAPDEN	WL + 4tCK + WR + 1tCK	89
Active	WRITEAP: BC4MRS		WL + 2tCK + WR + 1tCK	89
Idle	REFRESH	tREFPDEN	1tCK	90
Power-down	REFRESH	tXPDLL	Greater of 10tCK or 24ns	94
Idle	MODE REGISTER SET	tMRSPDEN	tMOD	93

Note : 1. If slow-exit mode precharge power-down is enabled and entered, ODT becomes asynchronous tANPD prior to CKE going LOW and remains asynchronous until tANPD + tXPDLL after CKE goes HIGH.

Entering power-down disables the input and output buffers, excluding CK, CK#, ODT, CKE, and RESET#. NOP or DES commands are required until tCPDED has been satisfied, at which time all specified input/output buffers are disabled. The DLL should be in a locked state when power-down is entered for the fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper READ operation as well as synchronous ODT operation.

During power-down entry, if any bank remains open after all in-progress commands are complete, the DRAM will be in active power-down mode. If all banks are closed after all in-progress commands are complete, the DRAM will be in precharge power-down mode. Precharge power-down mode must be programmed to exit with either a slow exit mode or a fast exit mode. When entering precharge power-down mode, the DLL is turned off in slow exit mode or kept on in fast exit mode.

The DLL also remains on when entering active power-down. ODT has special timing constraints when slow exit mode precharge power-down is enabled and entered. Refer to Asynchronous ODT Mode for detailed ODT usage requirements in slow exit mode precharge power-down. A summary of the two power-down modes is listed in Table 76.

While in either power-down state, CKE is held LOW, RESET# is held HIGH, and a stable clock signal must be maintained. ODT must be in a valid state but all other input signals are “Don’t Care.” If RESET# goes LOW during power-down, the DRAM will switch out of power-down mode and go into the reset state. After CKE is registered LOW, CKE must remain LOW until tPD (MIN) has been satisfied. The maximum time allowed for powerdown duration is tPD (MAX) (9 × tREFI).

The power-down states are synchronously exited when CKE is registered HIGH (with a required NOP or DES command). CKE must be maintained HIGH until tCKE has been satisfied. A valid, executable command may be applied after power-down exit latency, tXP, and tXPDLL have been satisfied. A summary of the power-down modes is listed below.

For specific CKE-intensive operations, such as repeating a power-down-exit-to-refresh to-power-down-entry sequence, the number of clock cycles between power-down exit and power-down entry may not be sufficient to keep the DLL properly updated. In addition to meeting tPD when the REFRESH command is used between power-down exit and power-down entry, two other conditions must be met. First, tXP must be satisfied before issuing the REFRESH command. Second, tXPDLL must be satisfied before the next power-down may be entered. An example is shown in Figure 94.

Table 76 : Power-Down Modes

DRAM State	MR0[12]	DLL State	Power-Down Exit	Relevant Parameters
Active (any bank open)	“Don’t Care”	On	Fast	^{t}XP to any other valid command
Precharged (all banks precharged)	1	On	Fast	^{t}XP to any other valid command
	0	Off	Slow	^{t}XPDLL to commands that require the DLL to be locked (READ, RDAP, or ODT on); ^{t}XP to any other valid command

Figure 84 : Active Power-Down Entry and Exit

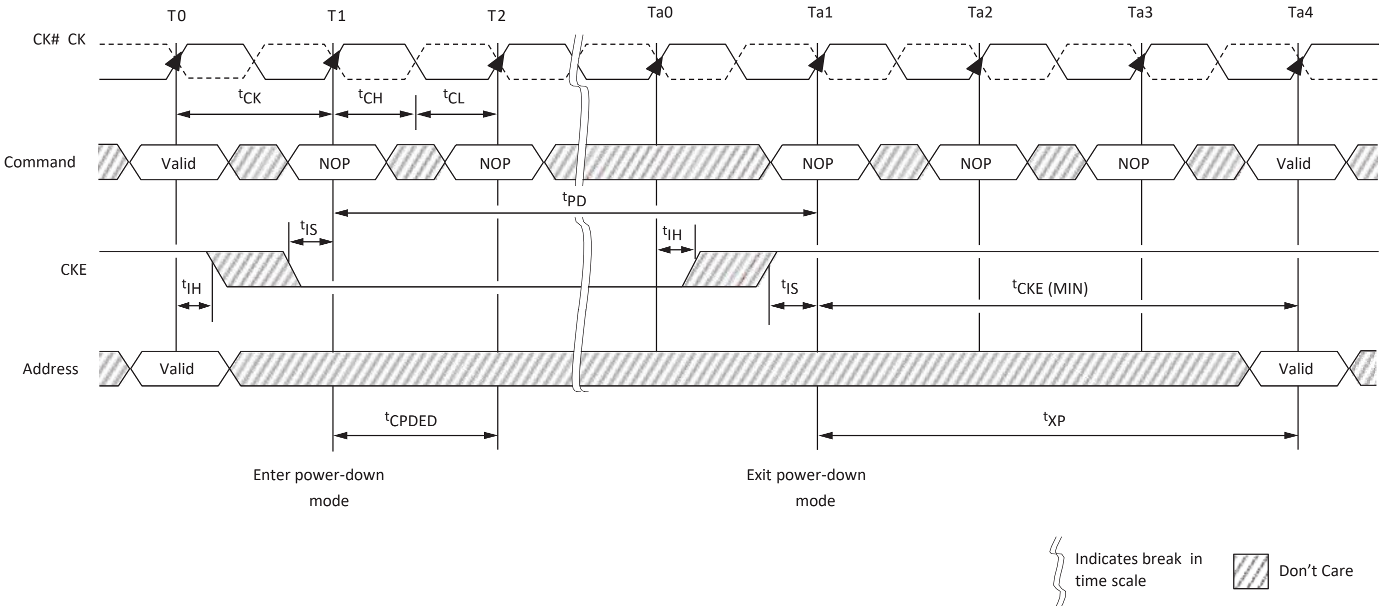


Figure 85 : Precharge Power-Down (Fast-Exit Mode) Entry and Exit

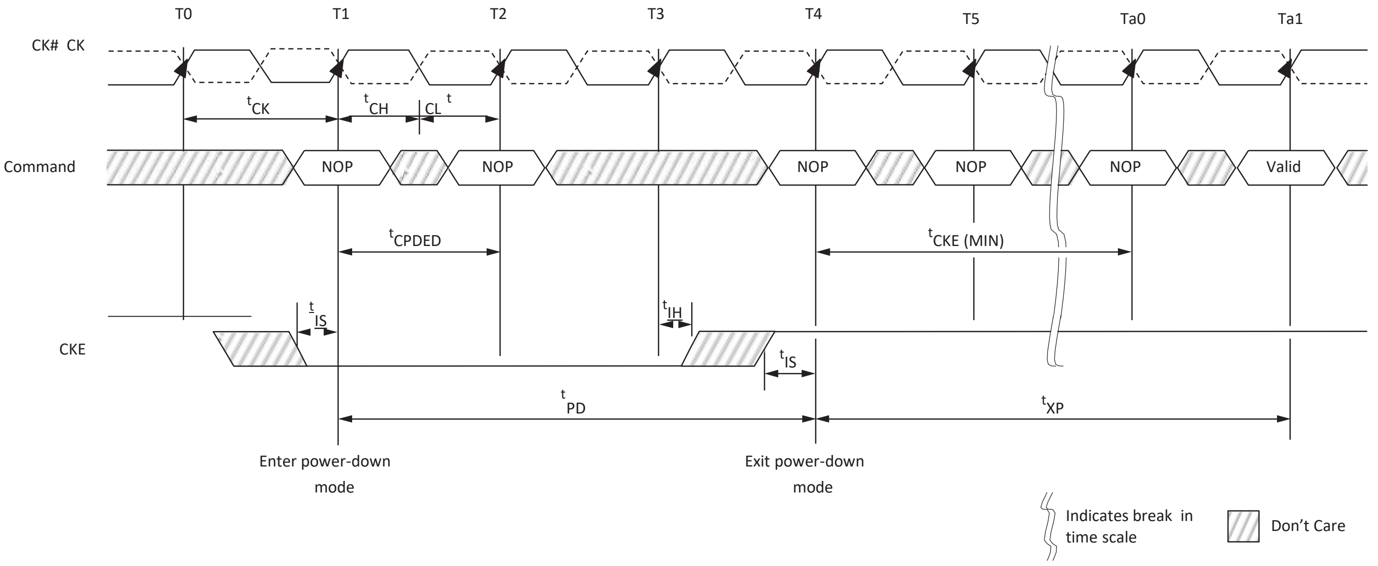
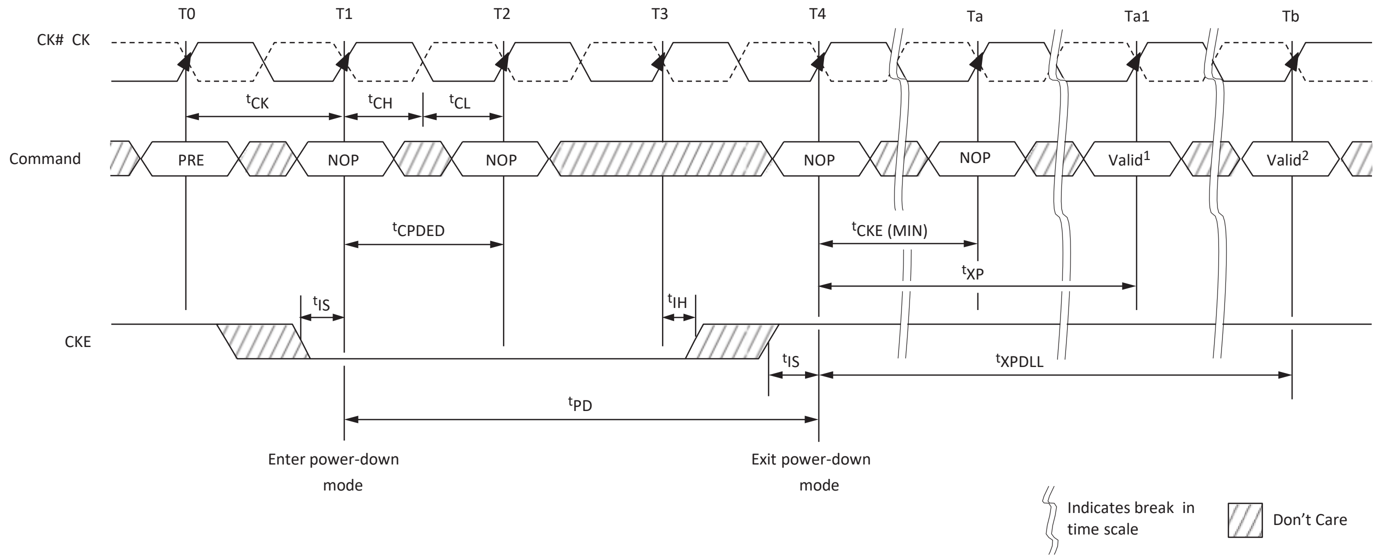


Figure 86 : Precharge Power-Down (Slow-Exit Mode) Entry and Exit



Notes: 1. Any valid command not requiring a locked DLL.
2. Any valid command requiring a locked DLL.

Figure 87 : Power-Down Entry After READ or READ with Auto Precharge (RDAP)

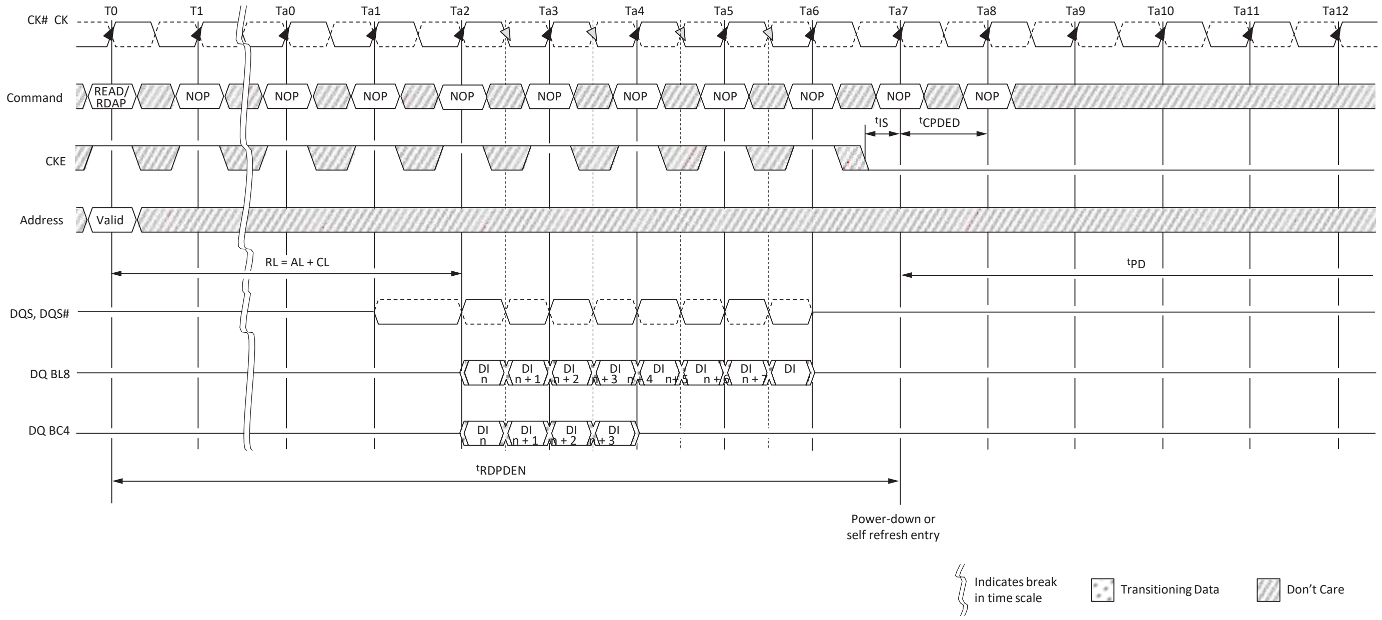
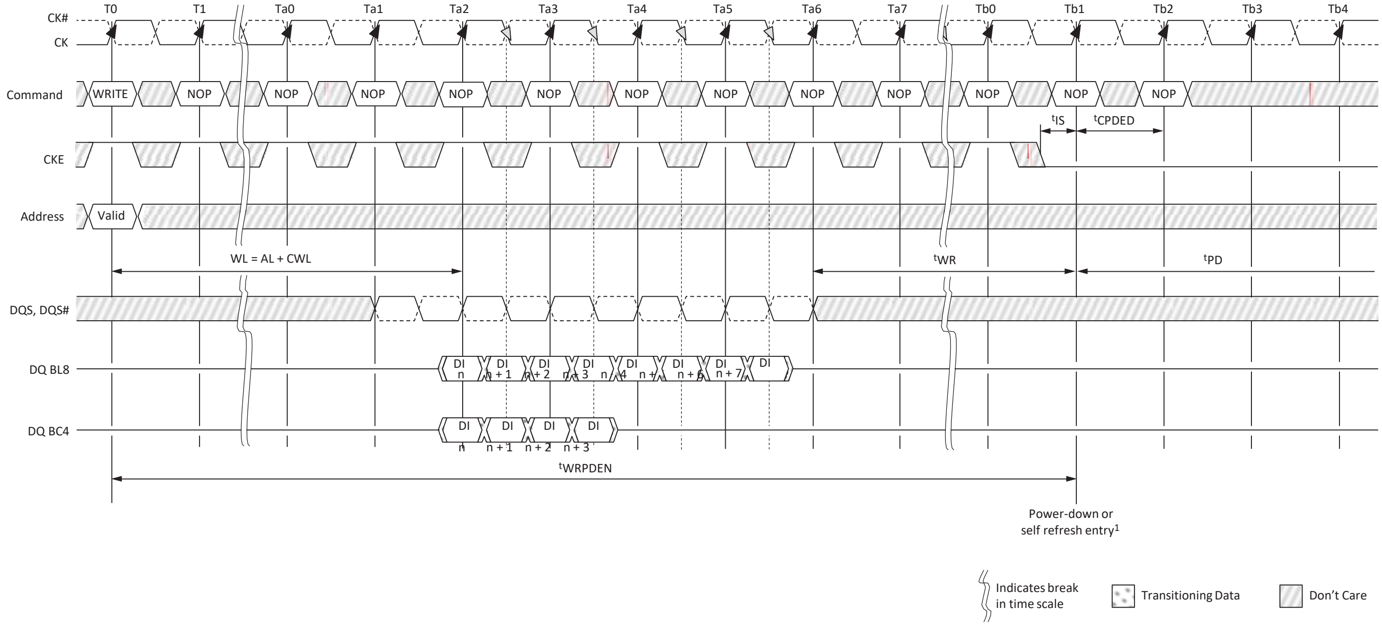
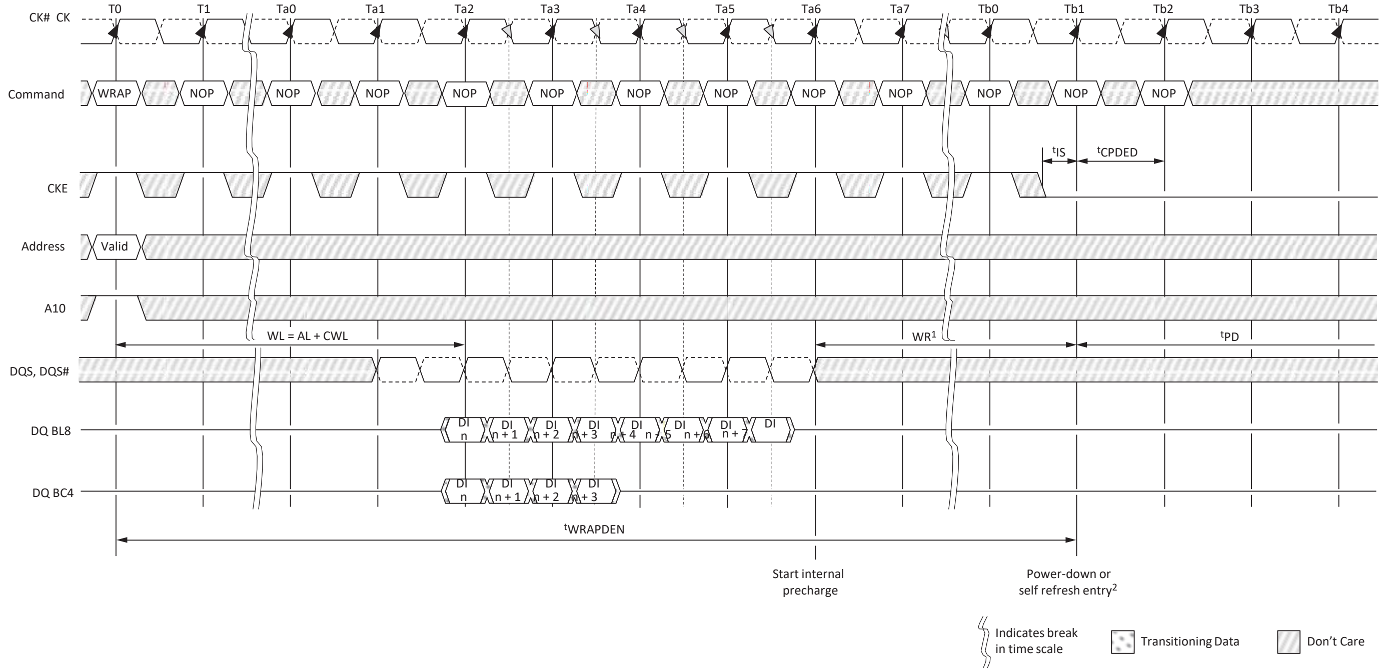


Figure 88 : Power-Down Entry After WRITE



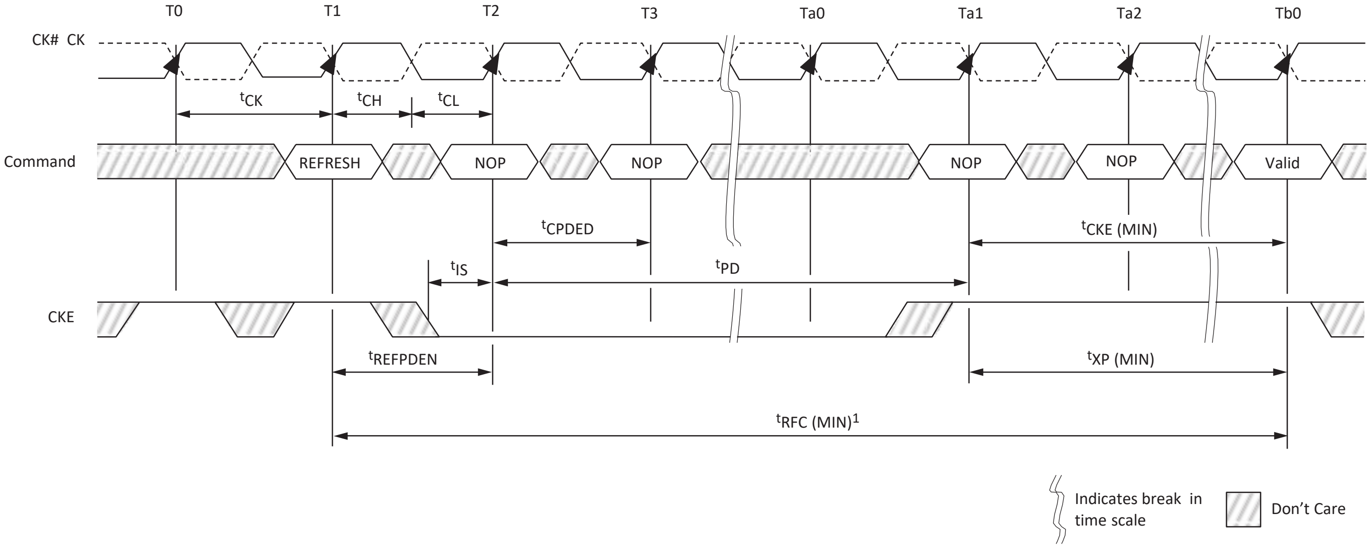
Note: 1. CKE can go LOW 2tCK earlier if BC4MRS.

Figure 89 : Power-Down Entry After WRITE with Auto Precharge (WRAP)



Notes: 1. tWR is programmed through MR0[11:9] and represents tWRmin (ns)/tCK rounded up to the next integer tCK.
2. CKE can go LOW 2tCK earlier if BC4MRS.

Figure 90 : REFRESH to Power-Down Entry



Note: 1. After CKE goes HIGH during tRFC, CKE must remain HIGH until tRFC is satisfied.

Figure 91 : ACTIVATE to Power-Down Entry

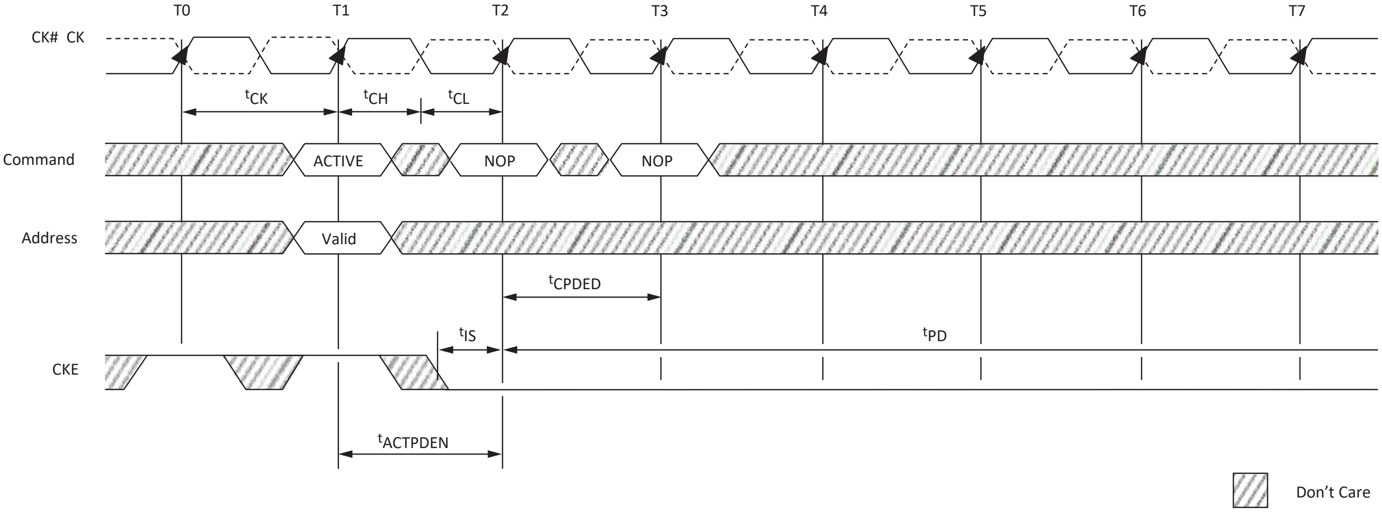


Figure 92 : PRECHARGE to Power-Down Entry

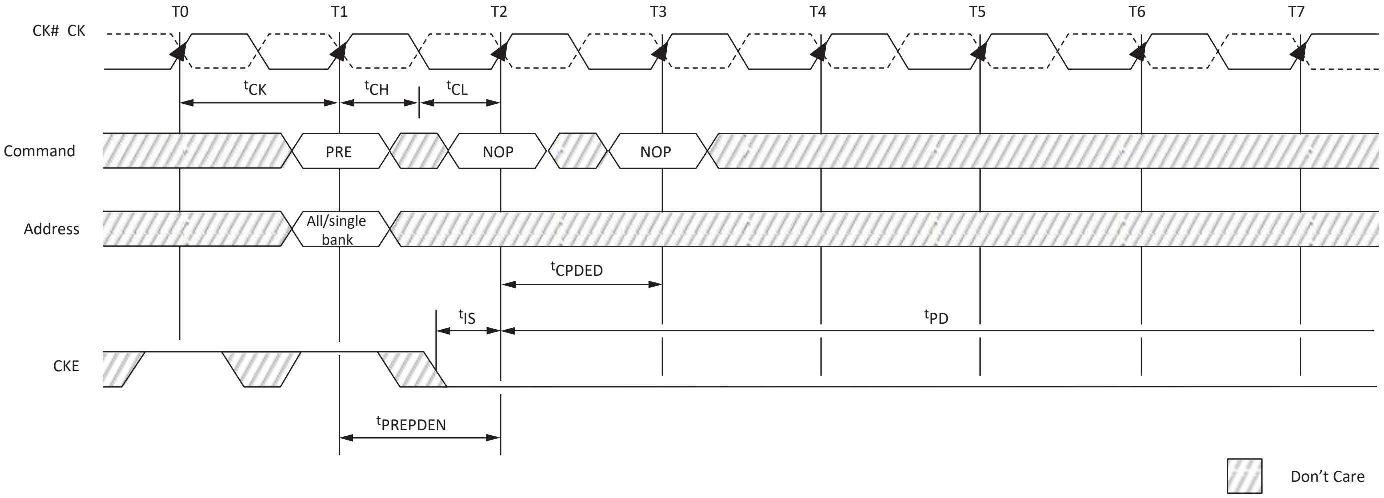


Figure 93 : MRS Command to Power-Down Entry

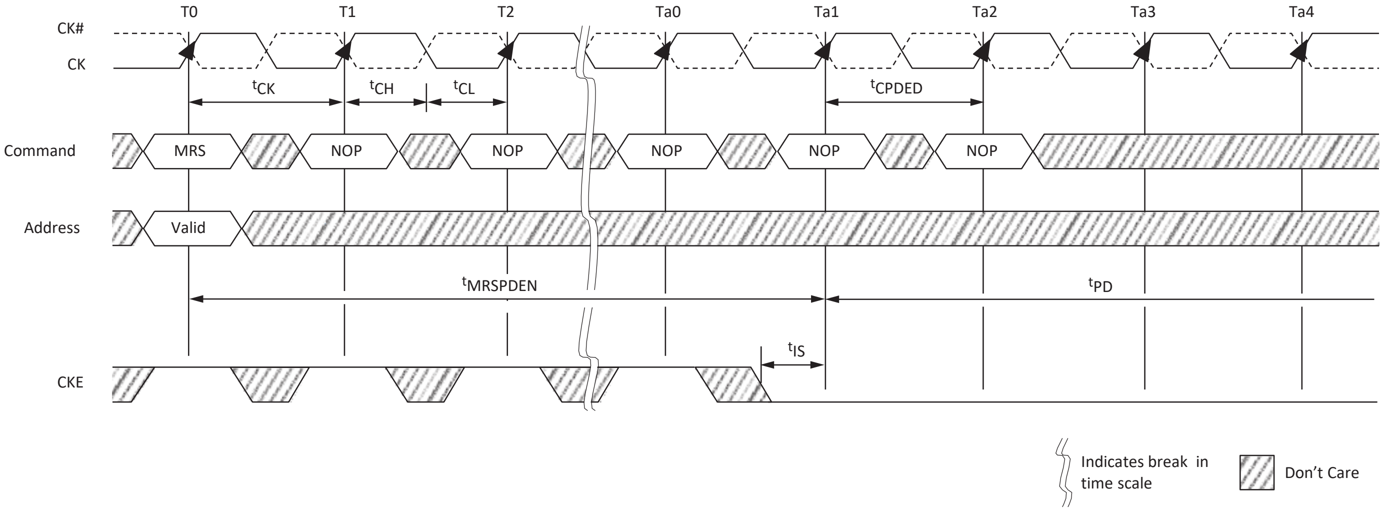
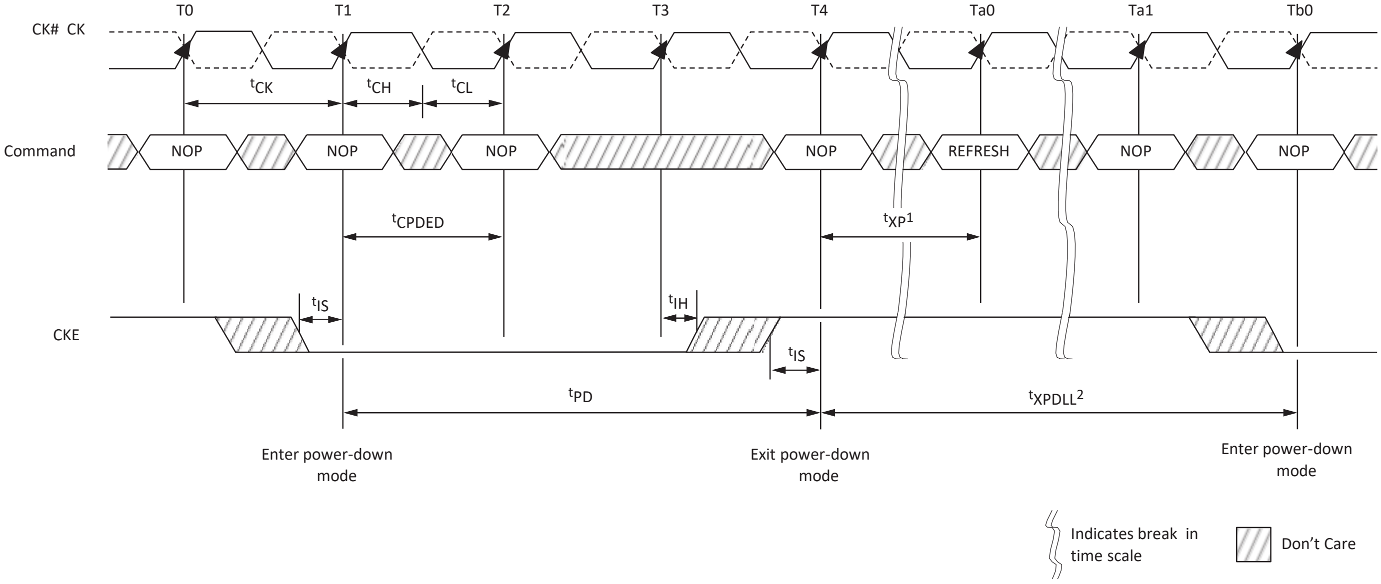


Figure 94 : Power-Down Exit to Refresh to Power-Down Entry



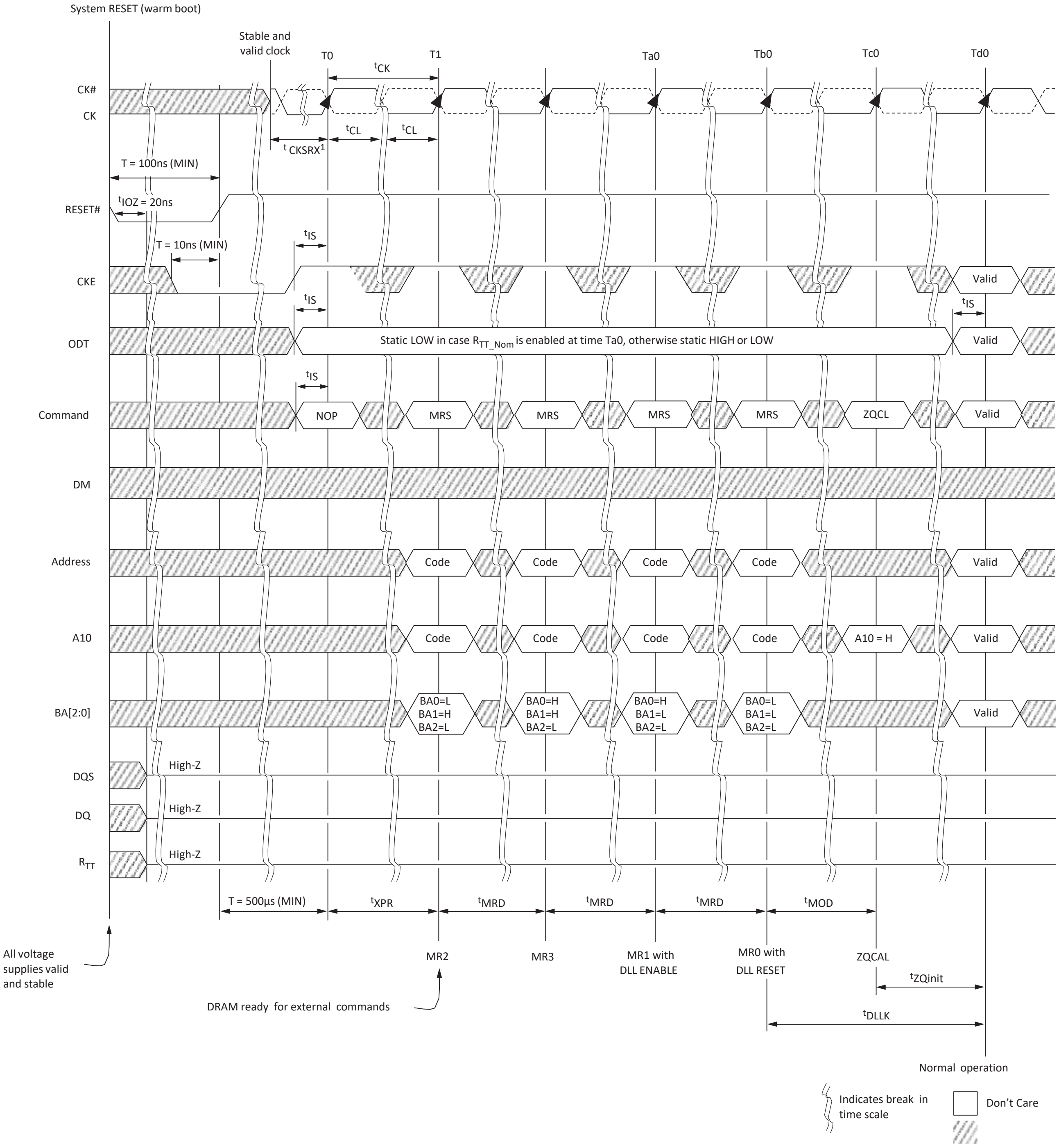
Notes: 1. tXP must be satisfied before issuing the command.

2. tXPDLL must be satisfied (referenced to the registration of power-down exit) before the next power-down can be entered.

RESET Operation

The RESET signal (RESET#) is an asynchronous reset signal that triggers any time it drops LOW, and there are no restrictions about when it can go LOW. After RESET# goes LOW, it must remain LOW for 100ns. During this time, the outputs are disabled, ODT (RTT) turns off (High-Z), and the DRAM resets itself. CKE should be driven LOW prior to RESET# being driven HIGH. After RESET# goes HIGH, the DRAM must be re-initialized as though a normal power-up was executed. All refresh counters on the DRAM are reset, and data stored in the DRAM is assumed unknown after RESET# has gone LOW.

Figure 95 : RESET Sequence



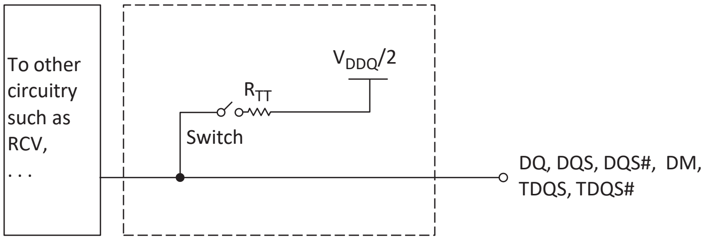
Note: 1. The minimum time required is the longer of 10ns or 5 clocks.

On-Die Termination (ODT)

On-die termination (ODT) is a feature that enables the DRAM to enable/disable and turn on/off termination resistance for each DQ, DQS, DQS#, and DM for the x4 and x8 configurations (and TDQS, TDQS# for the x8 configuration, when enabled). ODT is applied to each DQ, UDQS, UDQS#, LDQS, LDQS#, UDM, and LDM signal for the x16 configuration.

ODT is designed to improve signal integrity of the memory channel by enabling the DRAM controller to independently turn on/off the DRAM's internal termination resistance for any grouping of DRAM devices. ODT is not supported during DLL disable mode (simple functional representation shown below). The switch is enabled by the internal ODT control logic, which uses the external ODT ball and other control information.

Figure 96 : On-Die Termination



Functional Representation of ODT

The value of RTT (ODT termination resistance value) is determined by the settings of several mode register bits (see Table 81). The ODT ball is ignored while in self refresh mode (must be turned off prior to self refresh entry) or if mode registers MR1 and MR2 are programmed to disable ODT. ODT is comprised of nominal ODT and dynamic ODT modes and either of these can function in synchronous or asynchronous mode (when the DLL is off during precharge power-down or when the DLL is synchronizing). Nominal ODT is the base termination and is used in any allowable ODT state. Dynamic ODT is applied only during writes and provides OTF switching from no RTT or RTT,nom to RTT(WR).

The actual effective termination, RTT(EFF), may be different from RTT targeted due to nonlinearity of the termination. For RTT(EFF) values and calculations, see ODT Characteristics.

Nominal ODT

ODT (NOM) is the base termination resistance for each applicable ball; it is enabled or disabled via MR1[9, 6, 2] (see Mode Register 1 (MR1) Definition), and it is turned on or off via the ODT ball.

Table 77 : Truth Table – ODT (Nominal)

Note 1 applies to the entire table

MR1[9, 6, 2]	ODT Pin	DRAM Termination State	DRAM State	Notes
000	0	$R_{TT,nom}$ disabled, ODT off	Any valid	2
000	1	$R_{TT,nom}$ disabled, ODT on	Any valid except self refresh, read	3
000–101	0	$R_{TT,nom}$ enabled, ODT off	Any valid	2
000–101	1	$R_{TT,nom}$ enabled, ODT on	Any valid except self refresh, read	3
110 and 111	X	$R_{TT,nom}$ reserved, ODT on or off	Illegal	

Notes: 1. Assumes dynamic ODT is disabled (see Dynamic ODT) when enabled).
2. ODT is enabled and active during most writes for proper termination, but it is not illegal for it to be off during writes.
3. ODT must be disabled during reads. The RTT,nom value is restricted during writes. Dynamic ODT is applicable if enabled.

Nominal ODT resistance RTT,nom is defined by MR1[9, 6, 2], as shown in Mode Register 1 (MR1) Definition. The RTT,nom termination value applies to the output pins previously mentioned. DDR3 SDRAM supports multiple RTT,nom values based on RZQ/*n* where *n* can be 2, 4, 6, 8, or 12 and RZQ is 240Ω. RTT,nom termination is allowed any time after the DRAM is initialized, calibrated, and not performing read access, or when it is not in self refresh mode.

Write accesses use RTT,nom if dynamic ODT (RTT(WR)) is disabled. If RTT,nom is used during writes, only RZQ/2, RZQ/4, and RZQ/6 are allowed(see Table 81). ODT timings are summarized in Table 78, as well as listed in Table50.

Examples of nominal ODT timing are shown in conjunction with the synchronous mode of operation in Synchronous ODT Mode.

Table 78 : ODT Parameters

Symbol	Description	Begins at	Defined to	Definition for All DDR3 Speed Bins	Unit
ODTLon	ODT synchronous turn-on delay	ODT registered HIGH	$R_{TT(ON)}$ ± ^{t}AON	CWL + AL - 2	^{t}CK
ODTLoff	ODT synchronous turn-off delay	ODT registered HIGH	$R_{TT(OFF)}$ ± ^{t}AOF	CWL + AL - 2	^{t}CK
^{t}AONPD	ODT asynchronous turn-on delay	ODT registered HIGH	$R_{TT(ON)}$	2–8.5	ns
^{t}AOFPD	ODT asynchronous turn-off delay	ODT registered HIGH	$R_{TT(OFF)}$	2–8.5	ns
ODTH4	ODT minimum HIGH time after ODT assertion or write (BC4)	ODT registered HIGH or write registration with ODT HIGH	ODT registered LOW	4^{t}CK	^{t}CK
ODTH8	ODT minimum HIGH time after write (BL8)	Write registration with ODT HIGH	ODT registered LOW	6^{t}CK	^{t}CK
^{t}AON	ODT turn-on relative to ODTLon completion	Completion of ODTLon	$R_{TT(ON)}$	See Table 50	ps
^{t}AOF	ODT turn-off relative to ODTLoff completion	Completion of ODTLoff	$R_{TT(OFF)}$	0.5^{t}CK ± 0.2^{t}CK	^{t}CK

Dynamic ODT

In certain application cases, and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command, essentially changing the ODT termination on the fly. With dynamic ODT RTT(WR)) enabled, the DRAM switches from nominal ODT RTT,nom) to dynamic ODT RTT(WR)) when beginning a WRITE burst and subsequently switches back to nominal ODT RTT,nom) at the completion of the WRITE burst. This requirement is supported by the dynamic ODT feature, as described below.

Dynamic ODT Special Use Case

When DDR3 devices are architect as a single rank memory array, dynamic ODT offers a special use case: the ODT ball can be wired high (via a current limiting resistor preferred) by having RTT,nom disabled via MR1 and RTT(WR) enabled via MR2. This will allow the ODT signal not to have to be routed yet the DRAM can provide ODT coverage during write accesses.

When enabling this special use case, some standard ODT spec conditions may be violated : ODT is sometimes suppose to be held low. Such ODT spec violation (ODT not LOW) is allowed under this special use case. Most notably, if Write Leveling is used, this would appear to be a problem since RTT(WR) can not be used (should be disabled) and RTT(NOM) should be used. For Write leveling during this special use case, with the DLL locked, then RTT(NOM) maybe enabled when entering Write Leveling mode and disabled when exiting Write Leveling mode. More so, RTT(NOM) must be enabled when enabling Write Leveling, via same MR1 load, and disabled when disabling Write Leveling, via same MR1 load if RTT(NOM) is to be used.

ODT will turn-on within a delay of ODTLon + tAON + tMOD + 1CK (enabling via MR1) or turn-off within a delay of ODTLoff + tAOF + tMOD + 1CK. As seen in the table below, between the Load Mode of MR1 and the previously specified delay, the value of ODT is uncertain. this means the DQ ODT termination could turn-on and then turn-off again during the period of stated uncertainty.

Table 79 : Write Leveling with Dynamic ODT Special Case

Begin $R_{TT,nom}$ Uncertainty	End $R_{TT,nom}$ Uncertainty	I/Os	$R_{TT,nom}$ Final State
MR1 load mode command: Enable Write Leveling and $R_{TT(NOM)}$	ODTLon + ^{t}AON + ^{t}MOD + 1CK	DQS, DQS#	Drive $R_{TT,nom}$ value
		DQs	No $R_{TT,nom}$
MR1 load mode command: Disable Write Leveling and $R_{TT(NOM)}$	ODTLoff + ^{t}AOFF + ^{t}MOD + 1CK	DQS, DQS#	No $R_{TT,nom}$
		DQs	No $R_{TT,nom}$

Functional Description

The dynamic ODT mode is enabled if either MR2[9] or MR2[10] is set to 1. Dynamic ODT is not supported during DLL disable mode so RTT(WR) must be disabled. The dynamic ODT function is described below:

- Two RTT values are available—RTT,nom and RTT(WR).
  - The value for RTT,nom is preselected via MR1[9, 6, 2].
  - The value for RTT(WR) is preselected via MR2[10, 9].
- During DRAM operation without READ or WRITE commands, the termination is controlled.
  - Nominal termination strength RTT,nom is used.
  - Termination on/off timing is controlled via the ODT ball and latencies ODTLon and ODTLoff.
- When a WRITE command (WR, WRAP, WRS4, WRS8, WRAPS4, WRAPS8) is registered, and if dynamic ODT is enabled, the ODT termination is controlled.
  - A latency of ODTLcnw after the WRITE command: termination strength RTT,nom switches to RTT(WR)
  - A latency of ODTLcwn8 (for BL8, fixed or OTF) or ODTLcwn4 (for BC4, fixed or OTF) after the WRITE command : termination strength RTT(WR) switches back to RTT,nom.

– On/off termination timing is controlled via the ODT ball and determined by ODTLon, ODTLoff, ODTH4, and ODTH8.

– During the tADC transition window, the value of RTT is undefined.

ODT is constrained during writes and when dynamic ODT is enabled (see Table 80). ODT timings listed in Table 78 also apply to dynamic ODT mode.

Table 80 : Dynamic ODT Specific Parameters

Symbol	Description	Begins at	Defined to	Definition for All DDR3 Speed Bins	Unit
ODTLcnw	Change from $R_{TT,nom}$ to $R_{TT(WR)}$	Write registration	R_{TT} switched from $R_{TT,nom}$ to $R_{TT(WR)}$	WL - 2	^{t}CK
ODTLcwn4	Change from $R_{TT(WR)}$ to $R_{TT,nom}$ (BC4)	Write registration	R_{TT} switched from $R_{TT(WR)}$ to $R_{TT,nom}$	4^{t}CK + ODTL off	^{t}CK
ODTLcwn8	Change from $R_{TT(WR)}$ to $R_{TT,nom}$ (BL8)	Write registration	R_{TT} switched from $R_{TT(WR)}$ to $R_{TT,nom}$	6^{t}CK + ODTL off	^{t}CK
^{t}ADC	R_{TT} change skew	ODTLcnw completed	R_{TT} transition complete	0.5^{t}CK ± 0.2^{t}CK	^{t}CK

Table 81 : Mode Registers for RTT,nom

MR1 ($R_{TT,nom}$)			$R_{TT,nom}$ (RZQ)	$R_{TT,nom}$ (Ohm)	$R_{TT,nom}$ Mode Restriction
M9	M6	M2			
0	0	0	Off	Off	N/A
0	0	1	RZQ/4	60	Self refresh
0	1	0	RZQ/2	120	
0	1	1	RZQ/6	40	
1	0	0	RZQ/12	20	Self refresh, write
1	0	1	RZQ/8	30	
1	1	0	Reserved	Reserved	N/A
1	1	1	Reserved	Reserved	N/A

Note: 1. RZQ = 240Ω. If RTT,nom is used during WRITEs, only RZQ/2, RZQ/4, RZQ/6 are allowed.

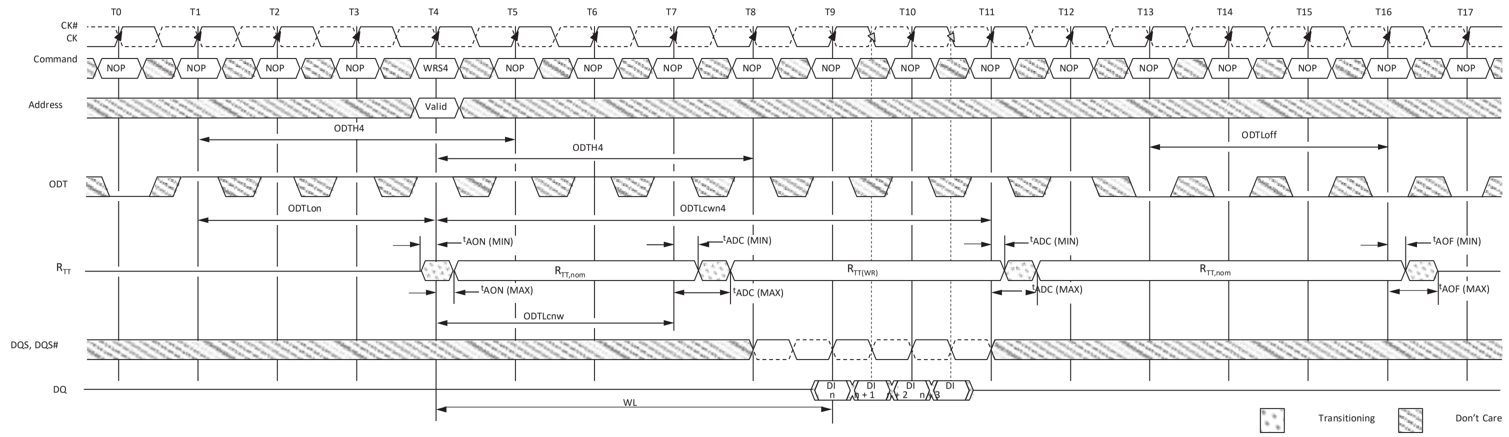
Table 82 : Mode Registers for RTT(WR)

MR2 ($R_{TT(WR)}$)		$R_{TT(WR)}$ (RZQ)	$R_{TT(WR)}$ (Ohm)
M10	M9		
0	0	Dynamic ODT off: WRITE does not affect $R_{TT,nom}$	
0	1	RZQ/4	60
1	0	RZQ/2	120
1	1	Reserved	Reserved

Table 83 : Timing Diagrams for Dynamic ODT

Figure and Page	Title
Figure 97	Dynamic ODT: ODT Asserted Before and After the WRITE, BC4
Figure 98	Dynamic ODT: Without WRITE Command
Figure 99	Dynamic ODT: ODT Pin Asserted Together with WRITE Command for 6 Clock Cycles, BL8
Figure 100	Dynamic ODT: ODT Pin Asserted with WRITE Command for 6 Clock Cycles, BC4
Figure 101	Dynamic ODT: ODT Pin Asserted with WRITE Command for 4 Clock Cycles, BC4

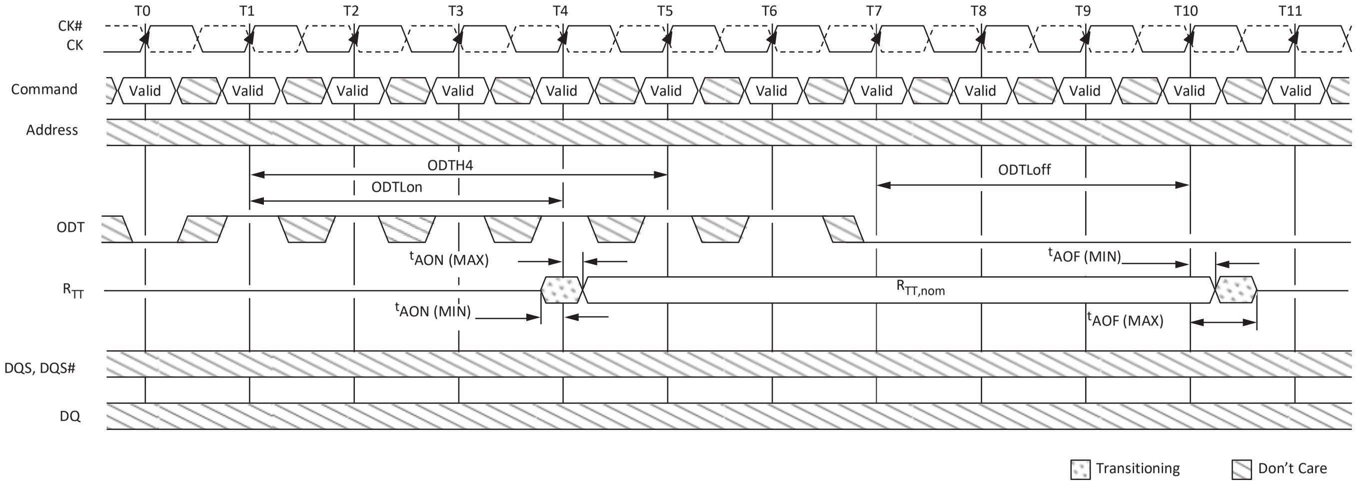
Figure 97 : Dynamic ODT: ODT Asserted Before and After the WRITE, BC4



Notes: 1. Via MRS or OTF. AL = 0, CWL = 5. RTT,nom and RTT(WR) are enabled.

2. ODTH4 applies to first registering ODT HIGH and then to the registration of the WRITE command. In this example, ODTH4 is satisfied if ODT goes LOW at T8 (four clocks after the WRITE command).

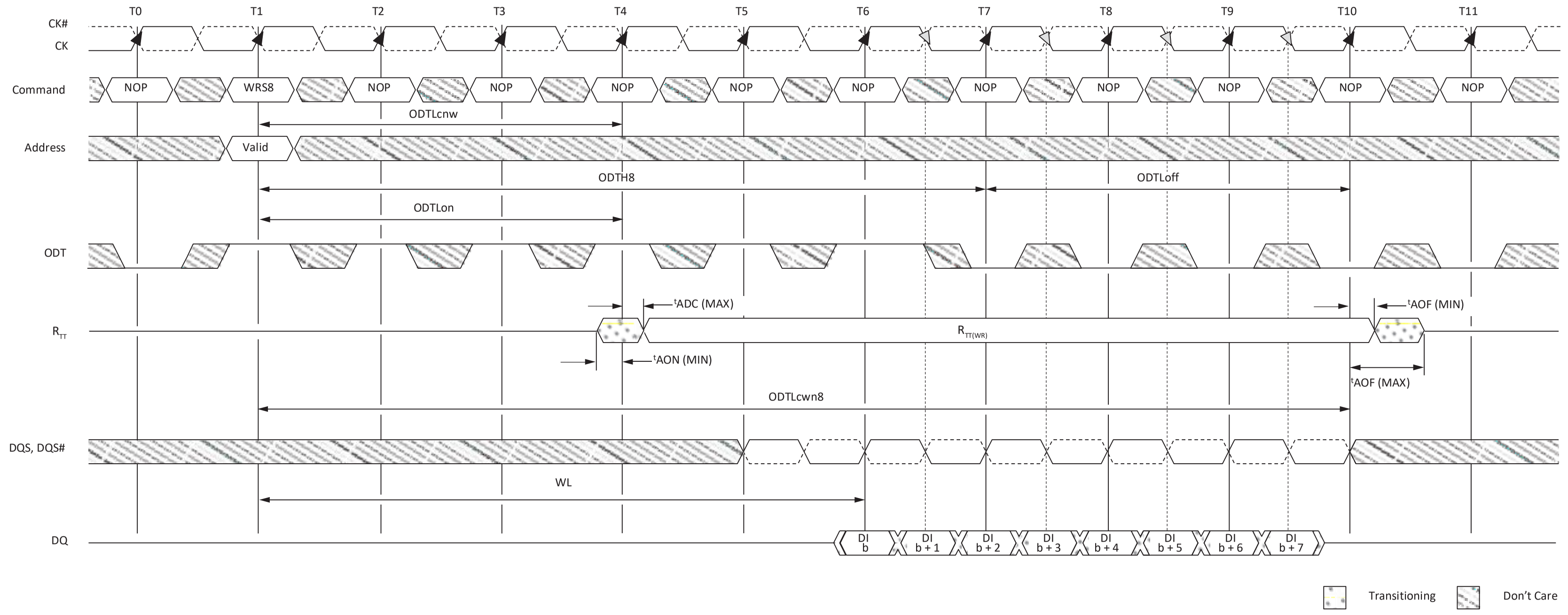
Figure 98 : Dynamic ODT: Without WRITE Command



Notes: 1. AL = 0, CWL = 5. RTT,nom is enabled and RTT(WR) is either enabled or disabled.

2. ODTH4 is defined from ODT registered HIGH to ODT registered LOW; in this example, ODTH4 is satisfied. ODT registered LOW at T5 is also legal.

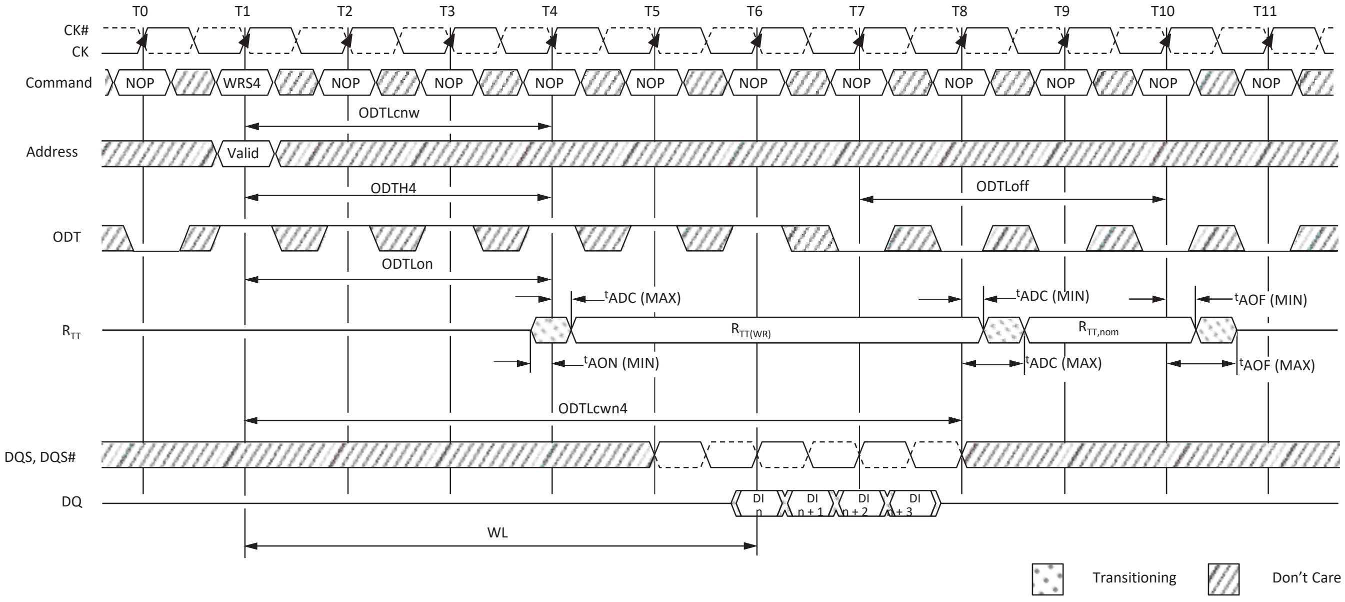
Figure 99 : Dynamic ODT: ODT Pin Asserted Together with WRITE Command for 6 Clock Cycles, BL8



Notes: 1. Via MRS or OTF; AL = 0, CWL = 5. If RTT,nom can be either enabled or disabled, ODT can be HIGH. RTT(WR) is enabled.

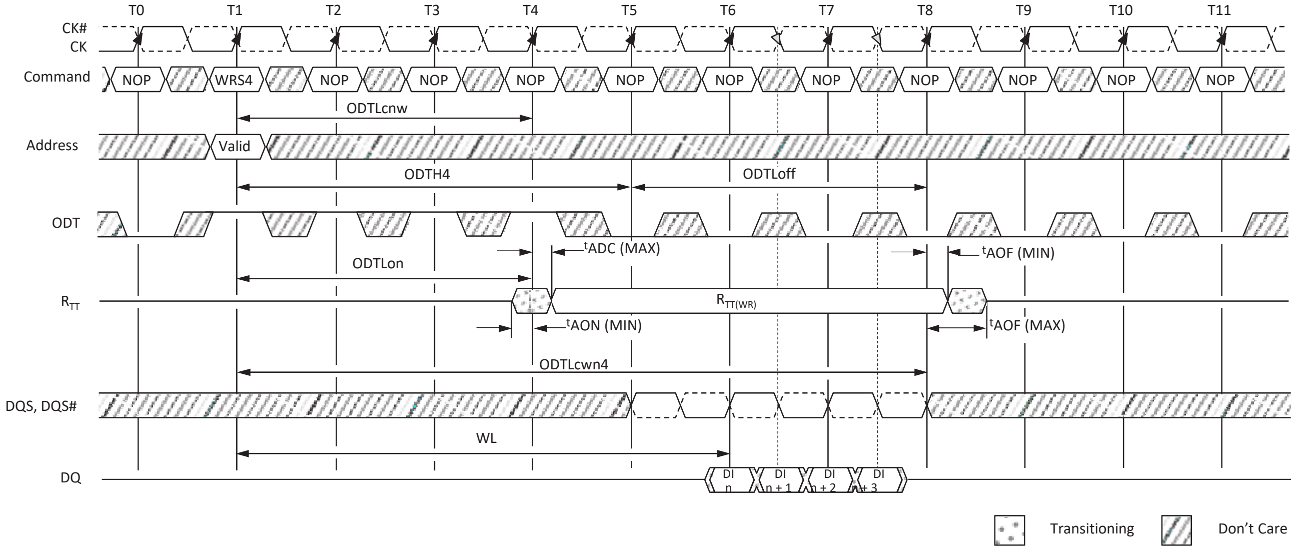
2. In this example, ODTH8 = 6 is satisfied exactly.

Figure 100 : Dynamic ODT: ODT Pin Asserted with WRITE Command for 6 Clock Cycles, BC4



Notes: 1. Via MRS or OTF. AL = 0, CWL = 5. RTT,nom and RTT(WR) are enabled.
2. ODTH4 is defined from ODT registered HIGH to ODT registered LOW, so in this example, ODTH4 is satisfied. ODT registered LOW at T5 is also legal.

Figure 101 : Dynamic ODT: ODT Pin Asserted with WRITE Command for 4 Clock Cycles, BC4



Notes: 1. Via MRS or OTF. AL = 0, CWL = 5. RTT,nom can be either enabled or disabled. If disabled, ODT can remain HIGH. RTT(WR) is enabled.
2. In this example ODTH4 = 4 is satisfied exactly.

Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked and when either RTT,nom or RTT(WR) is enabled. Based on the power-down definition, these modes are:

- Any bank active with CKE HIGH
- Refresh mode with CKE HIGH
- Idle mode with CKE HIGH
- Active power-down mode (regardless of MR0[12])
- Precharge power-down mode if DLL is enabled by MR0[12] during precharge powerdown

ODT Latency and Posted ODT

In synchronous ODT mode, RTT turns on ODTLon clock cycles after ODT is sampled HIGH by a rising clock edge and turns off ODTLoff clock cycles after ODT is registered LOW by a rising clock edge. The actual on/off times varies by tAON and tAOF around each clock edge (see Table 84). The ODT latency is tied to the WRITE latency (WL) by ODTLon = WL - 2 and ODTLoff = WL - 2.

Since write latency is made up of CAS WRITE latency (CWL) and additive latency (AL), the AL programmed into the mode register (MR1[4, 3]) also applies to the ODT signal. The device's internal ODT signal is delayed a number of clock cycles defined by the AL relative to the external ODT signal. Thus, ODTLon = CWL + AL - 2 and ODTLoff = CWL + AL - 2.

Timing Parameters

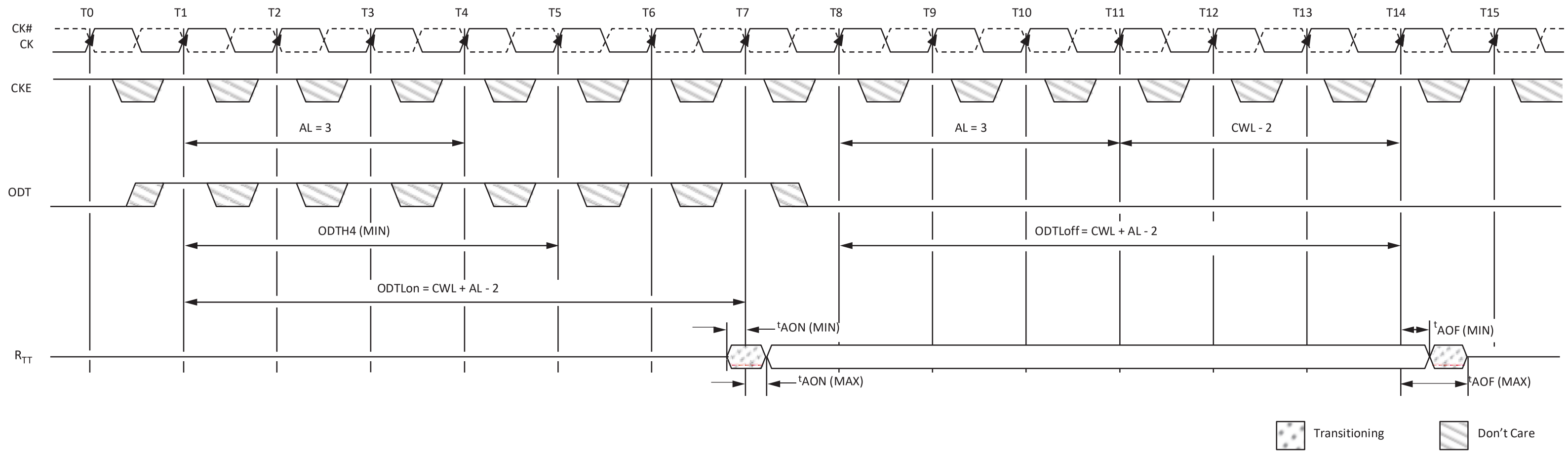
Synchronous ODT mode uses the following timing parameters: ODTLon, ODTLoff, ODTH4, ODTH8, tAON, and tAOF. The minimum RTT turn-on time (tAON [MIN]) is the point at which the device leaves High-Z and ODT resistance begins to turn on. Maximum RTT turn-on time (tAON [MAX]) is the point at which ODT resistance is fully on. Both are measured relative to ODTLon. The minimum RTT turn-off time (tAOF [MIN]) is the point at which the device starts to turn off ODT resistance. The maximum RTT turn off time (tAOF [MAX]) is the point at which ODT has reached High-Z. Both are measured from ODTLoff.

When ODT is asserted, it must remain HIGH until ODTH4 is satisfied. If a WRITE command is registered by the DRAM with ODT HIGH, then ODT must remain HIGH until ODTH4 (BC4) or ODTH8 (BL8) after the WRITE command (see Figure 103). ODTH4 and ODTH8 are measured from ODT registered HIGH to ODT registered LOW or from the registration of a WRITE command until ODT is registered LOW.

Table 84 : Synchronous ODT Parameters

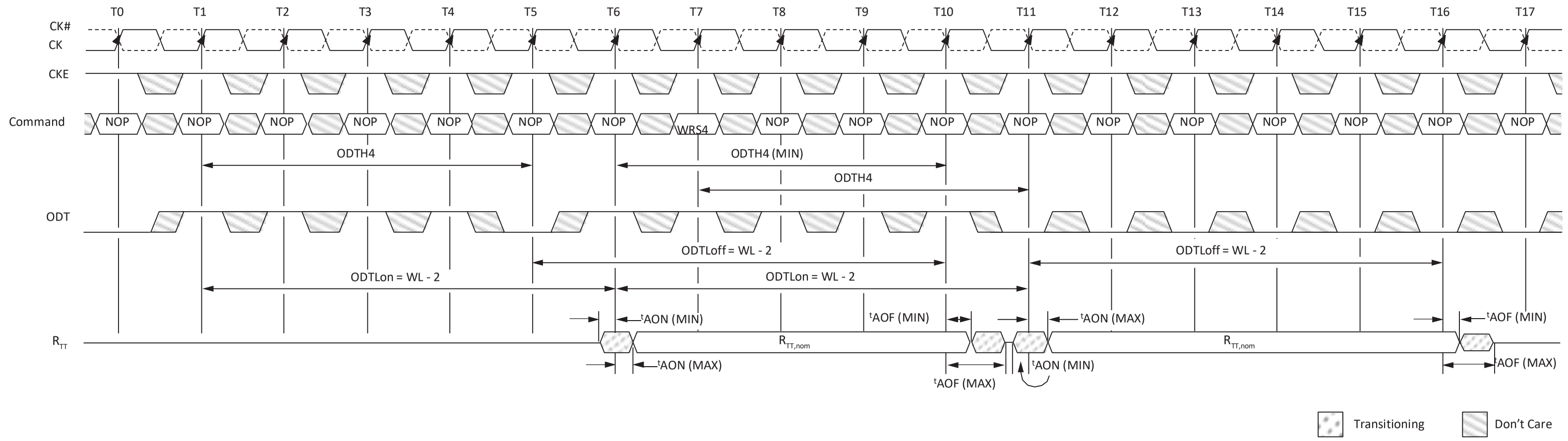
Symbol	Description	Begins at	Defined to	Definition for All DDR3 Speed Bins	Unit
ODTLon	ODT synchronous turn-on delay	ODT registered HIGH	$R_{TT(ON)}$ ±tAON	CWL + AL - 2	^{t}CK
ODTLoff	ODT synchronous turn-off delay	ODT registered HIGH	$R_{TT(OFF)}$ ±tAOF	CWL +AL - 2	^{t}CK
ODTH4	ODT minimum HIGH time after ODT assertion or WRITE (BC4)	ODT registered HIGH or write registration with ODT HIGH	ODT registered LOW	4^{t}CK	^{t}CK
ODTH8	ODT minimum HIGH time after WRITE (BL8)	Write registration with ODT HIGH	ODT registered LOW	6^{t}CK	^{t}CK
^{t}AON	ODT turn-on relative to ODTLon completion	Completion of ODTLon	$R_{TT(ON)}$	See Table 50	ps
^{t}AOF	ODT turn-off relative to ODTLoff completion	Completion of ODTLoff	$R_{TT(OFF)}$	0.5^{t}CK ± 0.2^{t}CK	^{t}CK

Figure 102 : Synchronous ODT



Note: 1. AL = 3; CWL = 5; ODTLon = WL = 6.0; ODTLoff = WL - 2 = 6. RTT,nom is enabled.

Figure 103 : Synchronous ODT (BC4)

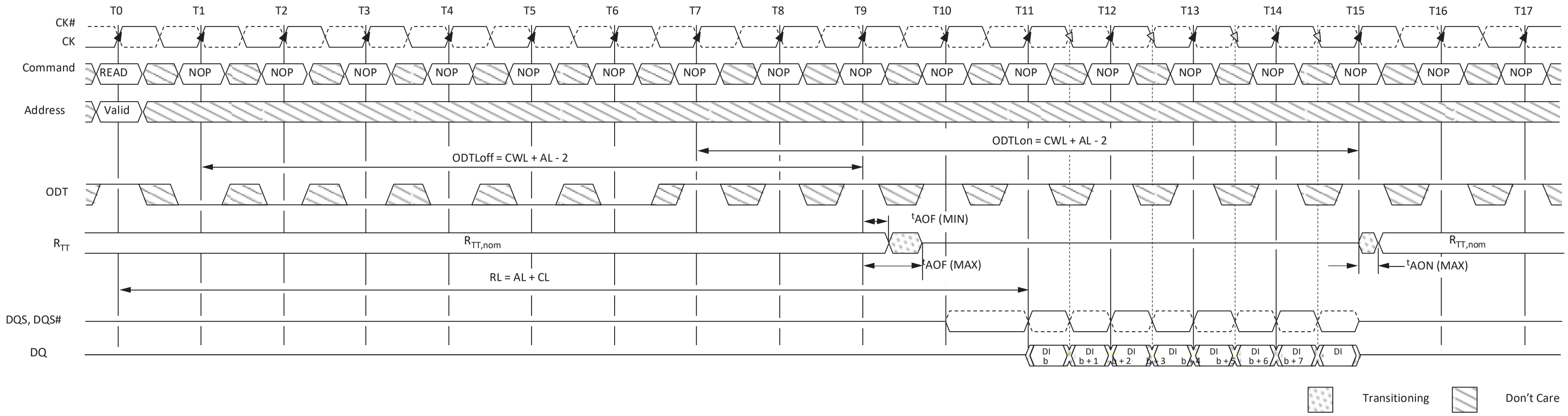


Notes: 1. WL = 7. RTT,nom is enabled. RTT(WR) is disabled.
2. ODT must be held HIGH for at least ODTH4 after assertion (T1).
3. ODT must be kept HIGH ODTH4 (BC4) or ODTH8 (BL8) after the WRITE command (T7).
4. ODTH is measured from ODT first registered HIGH to ODT first registered LOW or from the registration of the WRITE command with ODT HIGH to ODT registered LOW.
5. Although ODTH4 is satisfied from ODT registered HIGH at T6, ODT must not go LOW before T11 as ODTH4 must also be satisfied from the registration of the WRITE command at T7.

ODT Off During READs

Because the device cannot terminate and drive at the same time, RTT must be disabled at least one-half clock cycle before the READ preamble by driving the ODT ball LOW (if either RTT,nom or RTT(WR) is enabled).
RTT may not be enabled until the end of the postamble, as shown in the following example.
Note : ODT may be disabled earlier and enabled later than shown in Figure 104.

Figure 104 : ODT During READs



Note: 1. ODT must be disabled externally during READs by driving ODT LOW. For example, CL = 6; AL = CL - 1 = 5; RL = AL + CL = 11; CWL = 5; ODTLon = CWL + AL - 2 = 8; ODTLoff = CWL + AL - 2 = 8. RTT,nom is enabled. RTT(WR) is a “Don’t Care.”

Asynchronous ODT Mode

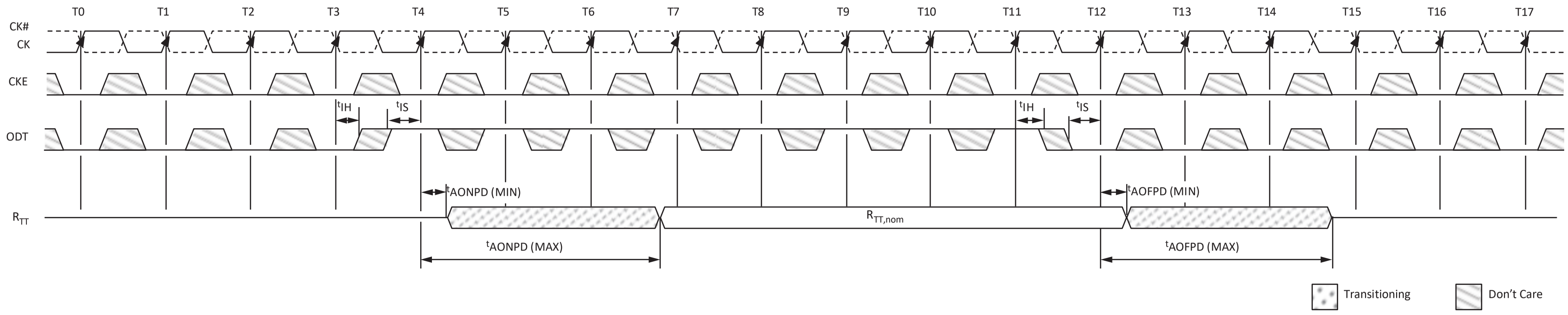
Asynchronous ODT mode is available when the DRAM runs in DLL on mode and when either $R_{TT,nom}$ or $R_{TT(WR)}$ is enabled; however, the DLL is temporarily turned off in pre- charged power-down standby (via MR0[12]). Additionally, ODT operates asynchronously when the DLL is synchronizing after being reset. See Power-Down Mode for definition and guidance over power-down details.

In asynchronous ODT timing mode, the internal ODT command is not delayed by AL relative to the external ODT command. In asynchronous ODT mode, ODT controls R_{TT} by analog time. The timing parameters ^{t}AONPD and ^{t}AOFPD replace ODTLon/^{t}AON and ODTLoff/^{t}AOF, respectively, when ODT operates asynchronously.

The minimum R_{TT} turn-on time (^{t}AONPD [MIN]) is the point at which the device termi- nation circuit leaves High-Z and ODT resistance begins to turn on. Maximum R_{TT} turn- on time (^{t}AONPD [MAX]) is the point at which ODT resistance is fully on. ^{t}AONPD (MIN) and ^{t}AONPD (MAX) are measured from ODT being sampled HIGH.

The minimum R_{TT} turn-off time (^{t}AOFPD [MIN]) is the point at which the device termi- nation circuit starts to turn off ODT resistance. Maximum R_{TT} turn-off time (^{t}AOFPD [MAX]) is the point at which ODT has reached High-Z. ^{t}AOFPD (MIN) and ^{t}AOFPD (MAX) are measured from ODT being sampled LOW.

Figure 105 : Asynchronous ODT Timing with Fast ODT Transition



Note: 1. AL is ignored.

Table 85 : Asynchronous ODT Timing Parameters for All Speed Bins

Symbol	Description	Min	Max	Unit
^{t}AONPD	Asynchronous R_{TT} turn-on delay (power-down with DLL off)	2	8.5	ns
^{t}AOFPD	Asynchronous R_{TT} turn-off delay (power-down with DLL off)	2	8.5	ns

Synchronous to Asynchronous ODT Mode Transition (Power-Down Entry)

There is a transition period around power-down entry (PDE) where the DRAM's ODT may exhibit either synchronous or asynchronous behavior. This transition period occurs if the DLL is selected to be off when in precharge power- down mode by the setting MR0[12] = 0. Power-down entry begins tANPD prior to CKE first being registered LOW, and ends when CKE is first registered LOW. tANPD is equal to the greater of ODTLoff + 1tCK or ODTLon + 1tCK. If a REFRESH command has been issued, and it is in progress when CKE goes LOW, power-down entry ends tRFC after the REFRESH command, rather than when CKE is first registered LOW. Power-down entry then becomes the greater of tANPD and tRFC - REFRESH command to CKE registered LOW.

ODT assertion during power-down entry results in an RTT change as early as the lesser of tAONPD (MIN) and ODTLon × tCK + tAON (MIN), or as late as the greater of tAONPD (MAX) and ODTLon × tCK + tAON (MAX). ODT de-assertion during power-down entry can result in an RTT change as early as the lesser of tAOFPD (MIN) and ODTLoff × tCK + tAOF (MIN), or as late as the greater of tAOFPD (MAX) and ODTLoff × tCK + tAOF (MAX). Table 86 summarizes these parameters.

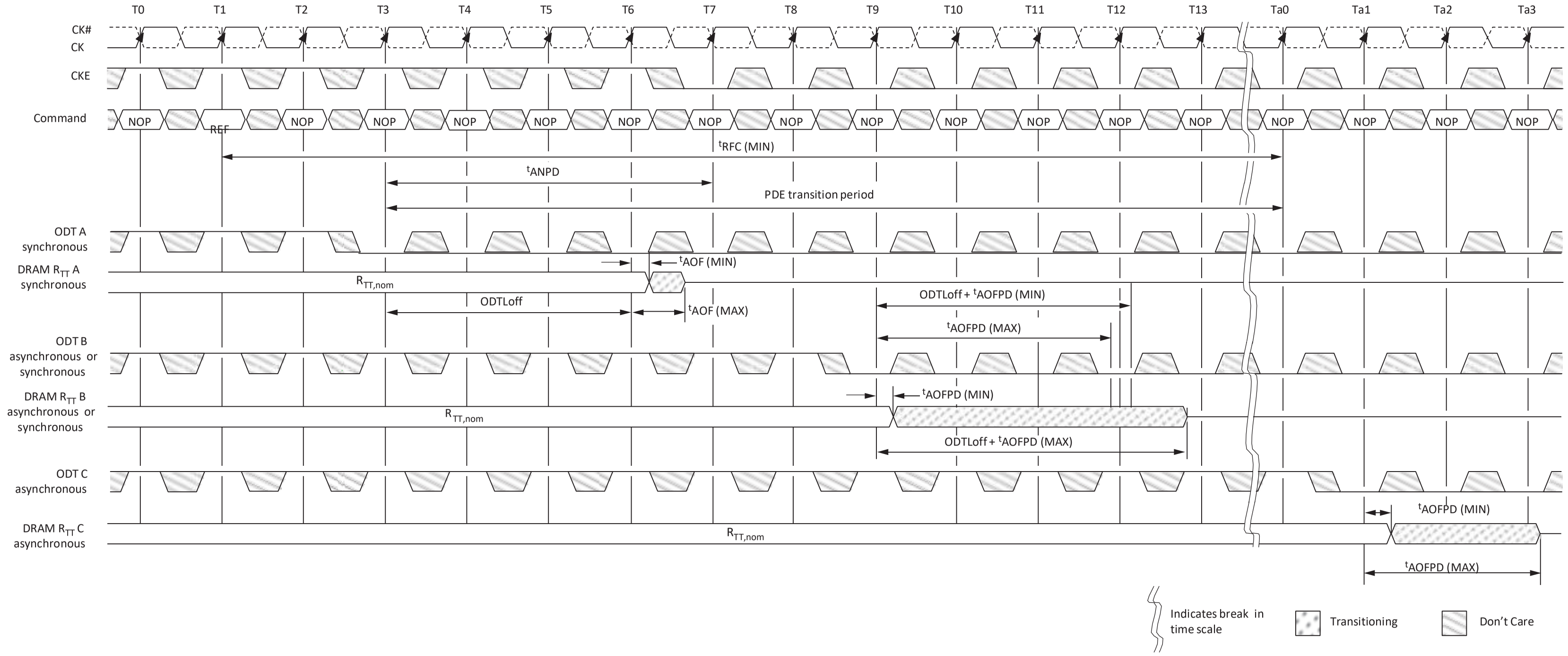
If AL has a large value, the uncertainty of the state of RTT becomes quite large. This is because ODTLon and ODTLoff are derived from the WL; and WL is equal to CWL + AL. Figure 106 shows three different cases:

- ODT_A: Synchronous behavior before tANPD.
- ODT_B: ODT state changes during the transition period with tAONPD (MIN) < ODTLon × tCK + tAON (MIN) and tAONPD (MAX) > ODTLon × tCK + tAON (MAX).
- ODT_C: ODT state changes after the transition period with asynchronous behavior.

Table 86 : ODT Parameters for Power-Down (DLL Off) Entry and Exit Transition Period

Description	Min	Max
Power-down entry transition period (power-down entry)	Greater of: ^{t}ANPD or ^{t}RFC - refresh to CKE LOW	
Power-down exit transition period (power-down exit)	^{t}ANPD + ^{t}XPDLL	
ODT to R_{TT} turn-on delay (ODTLon = WL - 2)	Lesser of: ^{t}AONPD (MIN) (2ns) or ODTLon × ^{t}CK + ^{t}AON (MIN)	Greater of: ^{t}AONPD (MAX) (8.5ns) or ODTLon × ^{t}CK + ^{t}AON (MAX)
ODT to R_{TT} turn-off delay (ODTLoff = WL - 2)	Lesser of: ^{t}AOFPD (MIN) (2ns) or ODTLoff × ^{t}CK + ^{t}AOF (MIN)	Greater of: ^{t}AOFPD (MAX) (8.5ns) or ODTLoff × ^{t}CK + ^{t}AOF (MAX)
^{t}ANPD	WL - 1 (greater of ODTLoff + 1 or ODTLon + 1)	

Figure 106 : Synchronous to Asynchronous Transition During Precharge Power-Down (DLL Off) Entry



Note: 1. AL = 0; CWL = 5; ODTL(off) = WL - 2 = 3.

Asynchronous to Synchronous ODT Mode Transition (Power-Down Exit)

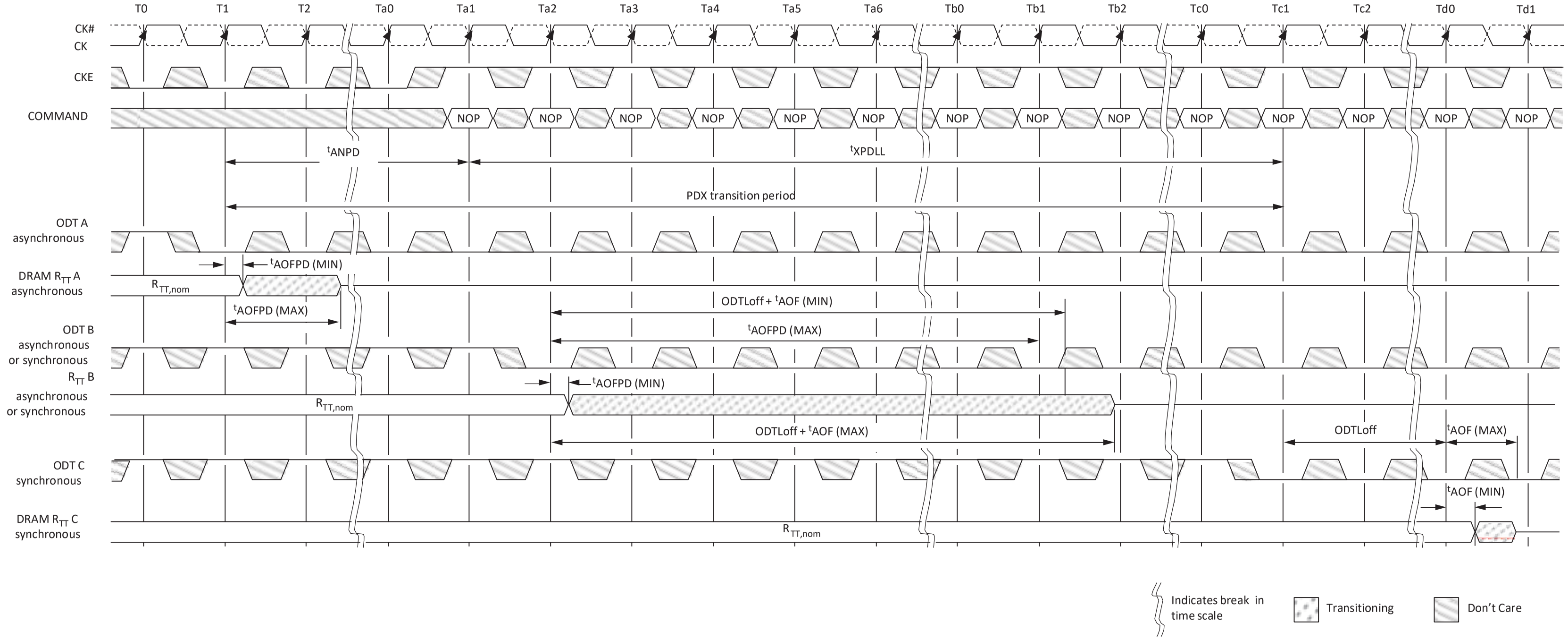
The DRAM's ODT can exhibit either asynchronous or synchronous behavior during power-down exit (PDX). This transition period occurs if the DLL is selected to be off when in precharge power-down mode by setting MR0[12] to 0. Power-down exit begins tANPD prior to CKE first being registered HIGH, and ends tXPDLL after CKE is first registered HIGH. tANPD is equal to the greater of ODTLoff + 1tCK or ODTLon + 1tCK. The transition period is tANPD + tXPDLL.

ODT assertion during power-down exit results in an RTT change as early as the lesser of tAONPD (MIN) and ODTLon × tCK + tAON (MIN), or as late as the greater of tAONPD (MAX) and ODTLon × tCK + tAON (MAX). ODT de-assertion during power-down exit may result in an RTT change as early as the lesser of tAOFPD (MIN) and ODTLoff × tCK + tAOF (MIN), or as late as the greater of tAOFPD (MAX) and ODTLoff × tCK + tAOF (MAX). Table 86 summarizes these parameters.

If AL has a large value, the uncertainty of the RTT state becomes quite large. This is because ODTLon and ODTLoff are derived from WL, and WL is equal to CWL + AL. Figure 107 shows three different cases :

- ODT C: Asynchronous behavior before tANPD.
- ODT B: ODT state changes during the transition period, with tAOFPD (MIN) < ODTLoff × tCK + tAOF (MIN), and ODTLoff × tCK + tAOF (MAX) > tAOFPD (MAX).
- ODT A: ODT state changes after the transition period with synchronous response.

Figure 107 : Asynchronous to Synchronous Transition During Precharge Power-Down (DLL Off) Exit



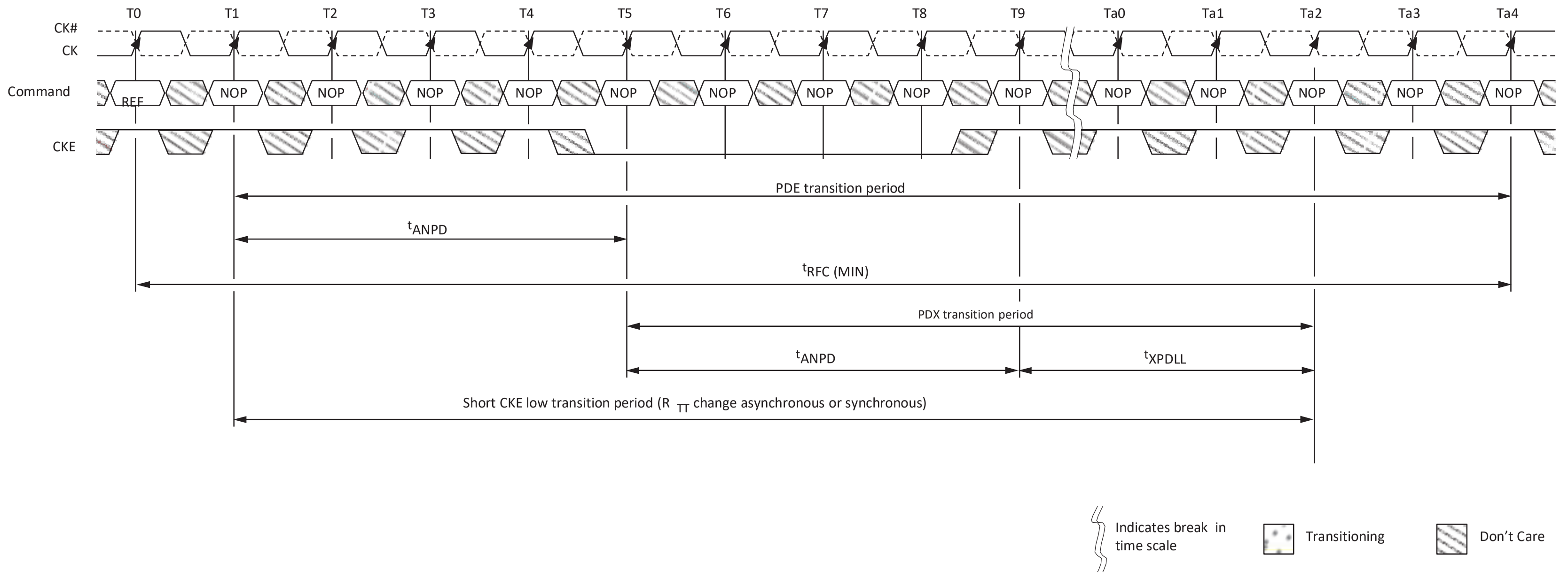
Note: 1. CL = 6; AL = CL - 1; CWL = 5; ODTLoff = WL - 2 = 8.

Asynchronous to Synchronous ODT Mode Transition (Short CKE Pulse)

If the time in the precharge power-down or idle states is very short (short CKE LOW pulse), the power-down entry and power-down exit transition periods overlap. When overlap occurs, the response of the DRAM's RTT to a change in the ODT state can be synchronous or asynchronous from the start of the power-down entry transition period to the end of the power-down exit transition period, even if the entry period ends later than the exit period.

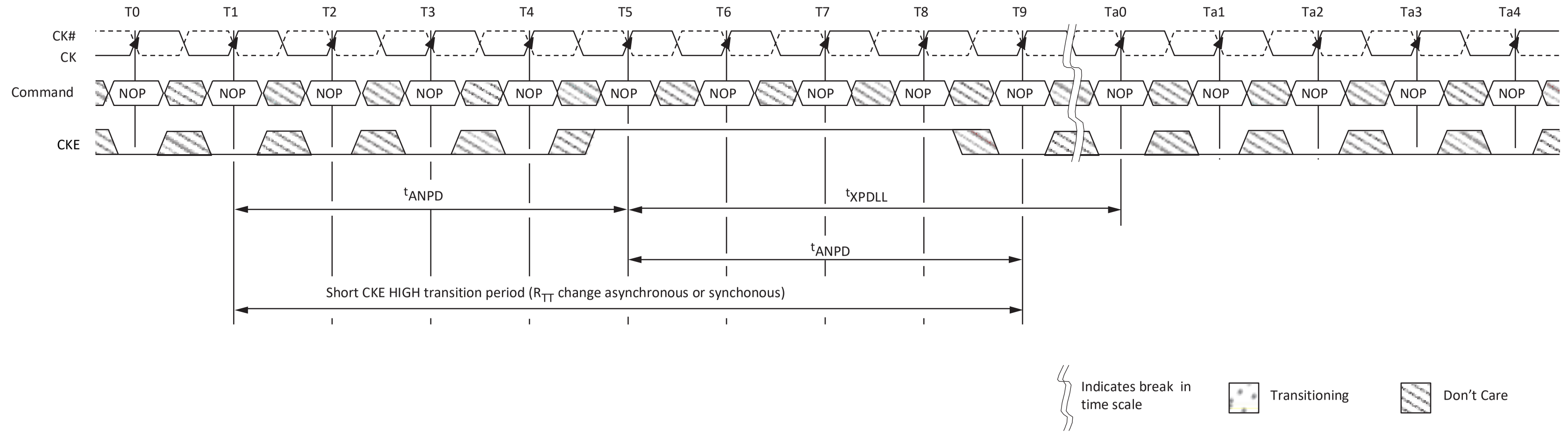
If the time in the idle state is very short (short CKE HIGH pulse), the power-down exit and power-down entry transition periods overlap. When this overlap occurs, the response of the DRAM's RTT to a change in the ODT state may be synchronous or asynchronous from the start of power-down exit transition period to the end of the powerdown entry transition period.

Figure 108 : Transition Period for Short CKE LOW Cycles with Entry and Exit Period Overlapping



Note: 1. AL = 0, WL = 5, tANPD = 4.

Figure 109 : Transition Period for Short CKE HIGH Cycles with Entry and Exit Period Overlapping



Note: 1. AL = 0, WL = 5, tANPD = 4.

Selection Guide

Part Number	VDD/VDDQ	I/O Width	Frequency	Data Rate	PKG TYPE
FM38D04SAA-5FFx	1.5V	X4	533Mhz	1066	78Ball FBGA
FM38D04SAA-6HFx	1.5V	X4	667Mhz	1333	78Ball FBGA
FM38D04SAA-8KFx	1.5V	X4	800Mhz	1600	78Ball FBGA
FM38D04SAA-9MFx	1.5V	X4	933Mhz	1866	78Ball FBGA
FM38D04SAA-ANFx	1.5V	X4	1067Mhz	2133	78Ball FBGA
FM38D08SAA-5FFx	1.5V	X8	533Mhz	1066	78Ball FBGA
FM38D08SAA-6HFx	1.5V	X8	667Mhz	1333	78Ball FBGA
FM38D08SAA-8KFx	1.5V	X8	800Mhz	1600	78Ball FBGA
FM38D08SAA-9MFx	1.5V	X8	933Mhz	1866	78Ball FBGA
FM38D08SAA-ANFx	1.5V	X8	1067Mhz	2133	78Ball FBGA
FM38D16SAB-5FFx	1.5V	X16	533Mhz	1066	96Ball FBGA
FM38D16SAB-6HFx	1.5V	X16	667Mhz	1333	96Ball FBGA
FM38D16SAB-8KFx	1.5V	X16	800Mhz	1600	96Ball FBGA
FM38D16SAB-9MFx	1.5V	X16	933Mhz	1866	96Ball FBGA
FM38D16SAB-ANFx	1.5V	X16	1067Mhz	2133	96Ball FBGA

Part Numbering System

FM 3 XX XX X X X - X X X X

Dosilicon Memory

Product Family
3 : Consumer DDR3 SDRAM

Device Depth
8D : 1G/8K ref

Organization
04 : x04
08 : x08
16 : x16

Interface
S : SSTL

Generation
A : 1st

Package Type
A : 78ball FBGA, 7.5x11mm^2, 1.2T max
B : 96ball FBGA, 7.5x13mm^2, 1.2T max

Clock Frequency(Data Rate)
5 : 533MHz(1066MHz)
6 : 667MHz(1333MHz)
8 : 800MHz(1600MHz)
9 : 933MHz(1866MHz)
A : 1067MHz(2133MHz)

CL-tRCD-tRP
D : 5-5-5
E : 6-6-6
F : 7-7-7
G : 8-8-8
H : 9-9-9
J : 10-10-10
K : 11-11-11
M : 13-13-13
N : 14-14-14

Power Supply
F : VDD/VDDQ=1.5V
G : VDD/VDDQ=1.35V

Temperature
B : -40℃~95℃
D : 0℃~95℃